Thesis for the Degree of Doctor of Philosophy in Engineering

Impact of adjacent dielectrics on the high-frequency performance of graphene field-effect transistors

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Cover: A schematic of graphene field-effect transistor on single crystal diamond substrate.

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Abstract

Transistors operating at high frequencies are the basic building blocks of millimeter wave communication and sensor systems. The high velocity and mobility of carriers in graphene can open ways for development of ultra-fast group IV transistors with similar or even better performance than that achieved with III-V based semiconductors. However, the progress of high-speed graphene transistors has been hampered by limitations associated with fabrication, influence of adjacent materials and self-heating effects.

This thesis work presents results of the comprehensive analysis of the influence of material imperfections, self-heating and limitations of the charge carrier velocity, imposed by adjacent dielectrics, on the transit frequency, f_{T}, and the maximum frequency of oscillation, f_{max}, of graphene field-effect transistors (GFETs). The analysis allowed for better understanding and developing a strategy for addressing the limitations.

In particular, it was shown that the GFET high-frequency performance can be enhanced by utilizing the gate and substrate dielectric materials with higher optical phonon (OP) energy, allowing for higher saturation velocity and, hence, higher f_{T} and f_{max}. This approach was experimentally verified by demonstration of enhancement in the f_{T} and f_{max} in GFETs with graphene channel encapsulated by the Al_2O_3 layers. As a further step, GFETs on diamond, material with highest OP energy and thermal conductivity, were introduced, developed and fabricated, showing the extrinsic f_{max} up to 50 GHz, at the gate length of 0.5 μm, which is highest reported so far among the best published graphene and semiconductor counterparts.

The main achievements of this thesis work are as follows: (i) comprehensive study of correlations between graphene-dielectric material quality, small-signal equivalent circuit parameters and high-frequency performance of the GFETs; (ii) experimental verification of the concept of improving the GFET high-frequency performance via selection of adjacent dielectric materials with high OP energy; (iii) introducing the diamond as a most promising dielectric material for high-frequency GFETs; (iv) development of technology and demonstration of fully integrated X and Ku band GFET IC amplifiers with state-of-the art performance.

In conclusion, the routes of future development depicted in this thesis work may allow for enhancing the high-frequency performance of GFETs up to the level or even higher than that of the modern III-V semiconductor counterparts.
Keywords: Graphene, field-effect transistors, high-frequency electronics, transit frequency, maximum frequency of oscillation, contact resistance, drift velocity, saturation velocity, diamond.

List of publications

Appended papers

This thesis is based on the following papers:

[A] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, K. Jeppson, L. Banszerus, M. Otto, C. Stampfer, D. Neumaier and J. Stake, "The dependence of the high-frequency performance of graphene field-effect transistors on channel transport properties", *IEEE J. Electron Devices Society*, 8, 457–464, 2020, doi: 10.1109/JEDS.2020.2988630.

[B] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier and J. Stake, "Graphene field-effect transistors with high extrinsic f_{T} and f_{max}", *IEEE Electron Device Letters,* 40, 131-134, 2019, doi: 10.1109/LED.2018.2884054.

[C] M. Asad, K. Jeppson, A. Vorobiev, M. Bonmann, J. Stake "Enhanced High-Frequency Performance of Top-Gated Graphene FETs Due to Substrate-Induced Improvements in Charge Carrier Saturation Velocity", *IEEE Transactions on Electron Devices,* 68, 899-902, 2021, doi: 10.1109/TED.2020.3046172.

[D] M. Asad, S. Majdi, A. Vorobiev, K. Jeppson, J. Isberg and J. Stake "Graphene FET on diamond for high frequency electronics", *Manuscript*, May 2021.

[E] P. C. Feijoo, F. Pasadas, M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, D. Neumaier, J. Stake and D. Jim´enez. "Does carrier velocity saturation help to enhance f_{max} in graphene field-effect transistors?", *Nanoscale Advances,* 2, 4179–4186, 2020, doi: 10.1109/TED.2021.3074479.

[F] K. Jeppson, M. Asad, J. Stake "Mobility degradation and series resistance in graphene field-effect transistor", *IEEE Transactions on Electron Devices,* 2021, doi: 10.1039/c9na00733d.

[G] A. Gareeb, M. Asad, M. -D .Wei, A. Vorobiev, J. Stake and R. Negra "Integrated 10-GHz Graphene FET Amplifier", *Submitted to IEEE Journal of Microwaves,* May 2021.

Notations and abbreviations

Notations

C_{ds}	Drain-source capacitance
C_{gd}	Gate-drain capacitance
C_{ox}	Gate oxide capacitance per unit area
E_F	Fermi energy
E_g	Band gap energy
E_{int}	Intrinsic electric field
E	Applied electric field
f_{max}	Extrinsic maximum frequency of oscillation
f_T	Extrinsic transit frequency
$f_{max-int}$	Intrinsic maximum frequency of oscillation
f_{T-int}	Intrinsic transit frequency
g_{ds}	Drain conductance
g_m	Transconductance
h	Planck's constant
h_{21}	Current gain
$\hbar$	Reduced Planck's constant
j_D	Drain current density
k_B	Boltzmann's constant
L_d	Drain conductance
L	Gate length
L_{acc}	Access length
m^*	Carrier effective mass
μ_0	Low field mobility
μ_{eff}	Effective mobility
n	Total carrier concentration
n_0	Residual carrier concentration
n_{eff}	Effective carrier concentration
$n_{m,doping}$	Metal induced doping concentration
n_{mg}	Carrier concentration in graphene under the metal
p	Hole concentration
q	Elementary charge
R	Resistance
R_C	Total source and drain series resistance

R_{mg}	Metal-graphene junction resistance
R_{ung}	Ungated contact resistance
R_D	Drain parasitic resistance
R_{DS}	Drain to source channel resistance
R_G	Gate resistance
R_i	Intrinsic gate source resistance
R_{pd}	Drain pad resistance
R_{pg}	Gate pad resistance
R_S	Source parasitic resistance
R_{sh}	Sheet resistance
ρ_C	Specific width contact resistivity
σ_C	Conductivity
σ_{min}	Minimum conductivity
τ	Scattering time
τ_{int}	Intrinsic transit time
U	Mason's unilateral gain
V_{Dir}	Dirac voltage
V_{DS}	Drain to source voltage
v_d	Drift carrier velocity
v_F	Fermi velocity
V_G	Gate voltage
v_{sat}	Saturation velocity
W	Gate width

Abbreviations

Al_2O_3	Aluminum oxide
Al	Aluminum
Au	Gold
BOE	Buffer oxide etchant
BP	Black phosphorus
Cu	Copper
CVD	Chemical vapor deposition
CNT	Carbon nanotube
DLC	Diamond-like carbon
FET	Field-effect transistor
FOM	Figure of merit
FWHM	Full width at half maximum
GaAs	Gallium arsenide
GFET	Graphene field-effect transistor
GHz	Gigahertz
hBN	Hexagonal boron nitride
HEMT	High electron mobility transistor
HBT	Heterojunction bipolar transistor
IC	Integrated circuit
InP	Indium phosphide
LNA	Low noise amplifier

MAG	Maximum available gain
MESFET	Metal-semiconductor field-effect transistor
MoS_2	Molybdenum disulfide
Ni	Nickel
OP	Optical phonon
Pd	Palladium
Pt	Platinum
RF	Radio frequency
SEM	Scanning electron microscope
SiO_2	Silicon dioxide
$SrTiO_3$	Strontium titanate
T	Temperature
THz	Terahertz
Ti	Titanium
TLM	Transfer length method
Si	Silicon

Contents

Chapter 1

Introduction

Ever since the very first field-effect transistor was fabricated by Shockley and Morgan in the Bell Labs [1], it brought revolution in semiconductor electronic technology. Transistors are the basis of all electronic equipment that is the part of our routine life, including computers, radios, mobile phones, displays, sensors and more. Continuous effort on scaling down the transistors to miniaturise the electronic equipment for the ease of consumers, resulted in new device concepts like laptops, tablets, smartphones and other handheld devices. The number of users of wireless devices has increased over the years. According to recent statistics, the number of mobile users worldwide at the end of 2020 has reached almost 5 billion, which means that billions of devices are connected through the Internet and exchange vast amounts of information in the form of text messages, pictures and videos with very high data rates [2]. With the current 4G technology, today's wireless networks operate at hundreds to thousands of Mbit/sec. The ongoing and upcoming 5G-6G revolution, is expected to connect billions more devices through Internet and wireless connections which operate at multi-Gbit/sec [3, 4]. All of these advancements in wireless communications is demanding high efficiency and bandwidth from the analog/radio frequency (RF) components. To cope with increasingly high data rates, it is necessary to develop analog front-ends of communication systems with high-speed transistors operating in millimeter wave bands and allowing for multi-gigabit data rates.

Up till now, the RF electronics industry demands have been fulfilled by Si-based transistors such as Si metal–oxide–semiconductor field-effect transistors (MOSFETs), SiGe heterojunction bipolar transistors (HBTs) and III-V compound metal-semiconductor field-effect transistors (MESFETs) and high electron mobility transistors (HEMTs) [5, 6]. A general problem with current Si MOSFET and III-V HEMT technology is the continuous scaling down to meet the industrial demands, where field-effect transistors (FETs) have already reached their best performance, and no further significant improvement in performance can be expected in future [7]. One reason for this is the continuous development toward down-scaling led to extremely short gates, very thin gate dielectric, extremely thin channel thickness and, therefore, the related problems, such as short channel effects, low breakdown voltage, low operating voltage, large surface scattering and threshold voltage variations [5, 6, 8, 9].

Further advancement in RF electronics requires extremely small dimensions

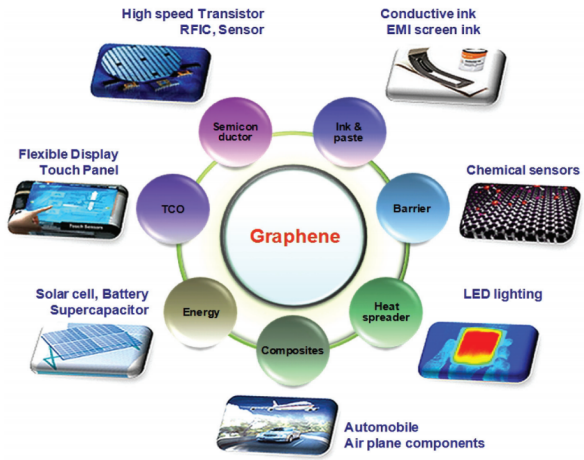


Figure 1.1: Scope of graphene in different research sectors [12].

and new material concepts. The choices are 2D materials such as graphene, Molybdenum disulfide (MoS_2) and black phosphorus (BP). These are the potential candidates for new channel materials for RF transistors. Graphene is a promising candidate for next generation of FETs for modern high-frequency applications. Graphene was first demonstrated by Andre Geim and Konstantin Novoselov in 2004 via separation from graphite by mechanical exfoliation [10,11]. Over the years, scientists have explored many applications of graphene in different areas of science as shown in Fig. 1.1 [12]. However, transistor which are used for high-speed/high-frequency applications require fast charge carriers in the channel, which can react quickly to an applied electric field.

Graphene has exceptional charge carrier transport properties with intrinsic high mobility over 10^5 cm^2/Vs at room temperature [13,14], which is 100 times higher than that of Si, and charge carriers saturation velocity 5×10^5 cm/s [15], which is about five times higher than that of Si. With these exciting features, graphene is a strong candidate for future RF electronics.

Attempts have been made realising graphene-based RF/microwave circuits such as frequency conversions [16,17], phase shifters [18], frequency multipliers [19,20], power detectors [21,22], rectifiers [23], as well as amplifiers [24–27]. One of the most appealing applications of graphene transistors are the amplifiers, which are yet challenging only by a few published studies [25,27,28]. The high-frequency performance of the FETs is usually characterised by the two main figures of merit (FOMs), the transit frequency f_T and the maximum frequency of oscillation f_{max}, defined as the frequencies at which current gain and unilateral power gain drop to unity, respectively. A comprehensive review study made by Frank Schweirz in 2013 on RF graphene field-effect transistors (GFET) shows that the f_T of GFET reveals scaling behaviour and even competes well with other conventional RF FETs [29]. On the other hand, the maximum frequency of oscillation f_{max}, which is an important FOM for RF analog front-ends, is reported to be consistently lower and does not scale with the gate length [29]. Analysis of previous studies indicates that the high-frequency performance in GFETs is limited by number of intrinsic and extrinsic factors [29–38]. The

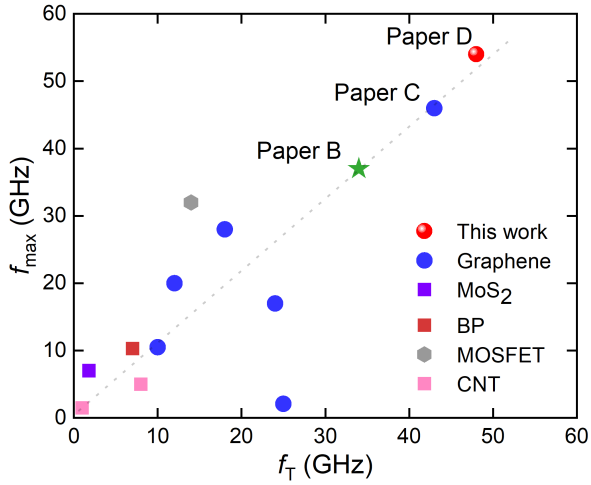


Figure 1.2: Benchmarking the different RF FET technologies by extrinsic maximum frequency of oscillation (f_{max}) and transit frequency (f_T) at similar gate lengths. Extrinsic f_{max} versus f_T of GFETs developed in this work is shown for 0.5 μm gate length [42, 43]. It is compared with other GFET using CVD, epitaxial and exfoliated graphene [30, 32, 35, 44, 45]. It is also compared with the FETs of other 2D materials including BP and MoS_2 [46, 47], CNT [48, 49] and MOSFET [50] at similar gate lengths.

intrinsic factor hindering realisation of competitive high-frequency GFETs is associated with zero-bandgap in monolayer graphene and, hence, lack of drain current saturation, which results in relatively high drain conductance (g_{ds}) and lower f_{max} [29]. An approach for addressing the issue by inducing bandgap in graphene turned out to be not promising, because it resulted in simultaneous reduction in the carrier mobility [29, 31, 39]. An alternative approach to address the high g_{ds} is the increase in the charge carrier velocity in GFETs by proper selection of the adjacent dielectric materials with relatively high optical phonons (OPs) energies [37, 40, 41].

Extrinsic limitations of the charge carrier transport in GFETs, degrading the high-frequency performance, are associated, mainly, with imperfections in graphene, interfaces and adjacent dielectrics, including the remote phonon scattering. In this thesis work, the focus was on addressing and overcoming the extrinsic limitations, which allowed for using efficiently the graphene superior electronic properties and enabling the high-frequency electronics applications. Fig. 1.2 shows the extrinsic f_{max} versus f_T reported in this work in comparison with other RF GFETs and RF transistors of 2D materials and carbon nanotube as well as MOSFETs for similar gate length. As it can be seen, this work represents state-of-the-art technology of high-frequency graphene field-effect transistors.

In this thesis work, first, efforts have been made for better understanding the high-frequency performance limitations caused by the graphene quality, see Paper [A]. The low-field carrier mobility was selected as the most appropriate material-quality parameter because of its combined response to different types of material imperfections. The correlations between low-field mobility and high-frequency performance of GFETs are observed, analysed and explained

by using and combining the semi-empirical models of drain resistance, charge carrier velocity, velocity saturation and small-signal equivalent circuits model. It was found that a promising approach for improving the GFET high-frequency performance is the selection of adjacent dielectric materials with OP energy higher than that of SiO_2, i.e. 55 meV, allowing for higher saturation velocity and, hence, higher f_T and f_{max}.

Paper [B] reports on GFETs still fabricated on SiO_2 substrate and with Al_2O_3 gate dielectric, but with improved quality of the graphene and adjacent dielectrics, which allowed for minimising emission of carriers from traps and, hence, achieving the drain current saturation trend following that of the velocity. This resulted in state-of-the-art extrinsic f_T and f_{max} up to 40 GHz at the 0.5 μm gate length, which is comparable or even better than those of the best published Si MOSFETs. However, f_T and f_{max} of the GFETs are still limited by the inelastic carrier-phonons interactions of the graphene and adjacent dielectrics. In this work, it was suggested replacing the SiO_2 by Al_2O_3 with higher OPs energy of 87 meV, since it can be readily realised with the developed technology.

The proposed concept of encapsulation of the graphene channel by dielectric layers with relatively high OP energy was realised experimentally in Paper [C]. The GFETs with Al_2O_3 gate dielectric and Al_2O_3 buffer layer between the graphene channel and SiO_2/Si substrate were fabricated and characterised. The GFETs reveals extrinsic f_T and f_{max} up to 43 and 46 GHz, respectively, at 0.5 μm gate length, which were again higher then those of the best published GFETs with similar gate length. Paper [E], presented in collaboration with Barcelona University, reports on comprehensive modelling of the charge carrier transport and high-frequency performance of GFETs presented in Paper [B]. In particular, it was shown that high thermal conductivity of substrate is a crucial property of GFETs for high-frequency applications. At relatively high drain fields, above approx. 1 V/μm, required for the carrier velocity saturation, the channel temperature in GFET on SiO_2/Si substrate can be as high as 600 K, due to intensive Joule heating provoked by the low thermal conductivity of the SiO_2 layer. The increase in the channel temperature induces thermally generated carriers, which result in the reduction of the saturation velocity and, hence, degradation of the f_T. On the other hand, it is shown that the above effect allows for relative saturation of the drain current resulting in reduced drain conductance and, hence enhanced f_{max}.

Paper [D] presents results of further development of the approach of enhancing the high-frequency performance of GFETs by selecting the adjacent dielectric materials with relatively high OP energy. Analysis indicates that most suitable candidate is the diamond, since its OPs energy can be as high as 165 meV, which is comparable with that of the graphene zone-edge OPs. In this case, the carrier velocity in GFETs is entirely defined by the intrinsic graphene OPs. The GFETs on diamond substrates were fabricated and characterised. The saturation velocity of $3.7 \cdot 10^7$ cm/s and state-of-the-art extrinsic f_T and f_{max} up to 55 GHz at 0.5 μm gate length, were demonstrated with promising scaling down behaviour. These f_T and f_{max} values are highest reported so far for GFETs with similar gate length. In Paper [F] a first-order mobility degradation model is used to separate information about mobility degradation and series resistance for a set of GFETs of different channel lengths. Mobility

degradation behaviour was observed for GFET devices with the mobility being reduced to half for a voltage-induced charge carrier density of 10^{13}cm^{-2}. The model is important for accurate extraction of parameters and characterising the GFETs.

Finally, Paper [G] presents the X and Ku band fully-integrated GFET IC amplifiers designed, in collaboration with Aachen University, fabricated and measured. The amplifiers utilise the GFETs with the state-of-the-art high-frequency performance developed and presented in Papers [A]-[D]. Peak gains of 4.2 dB and 2.9 dB at 10.6 GHz and 13.6 GHz were measured, respectively, for each GFET amplifier. The achieved gain values are higher than those reported so far for the GFET IC amplifiers.

The thesis outline is as follows. In chapter 2, graphene's electronic properties relevant for the high-frequency electronics applications are considered. Chapter 3 describes the specifics of the high-frequency GFET's designs, fabrication, DC and RF models and performances, as well as effects of the self-heating. In chapter 4, the effects of material imperfections on the high-frequency performance of GFETs are analysed. Chapter 5 describes the GFETs with enhanced high-frequency performance utilising dielectric materials with high optical phonon energy. Chapter 6 reviews current status of GFET IC amplifiers and presents the developed and fabricated Ku-band IC amplifier based on high performance GFETs. Finally, the thesis is concluded with a summary and future outlook.

Chapter 2

Transport properties of graphene

The analog front-ends of advanced communication systems require high speed transistors operating at mmWave frequencies and providing a large bandwidth. Two main figures of the merit of RF transistors are the f_{T} and f_{max}, and both depend on the charge carrier velocity in the channel. Thus, materials with high mobility and high charge carrier saturation velocity are required as channel material in order to realise such RF transistor devices. In this context, monolayer graphene is a promising candidate with intrinsically high mobility and charge carrier saturation velocity. This chapter describes the basic properties of graphene which make it qualified for high-frequency analog applications. The specific graphene properties such as V-shaped band structure, charge carrier density, material imperfections and low- and high-field charge carrier transport will be discussed. It begins with the quote of Nobel laureate Andre Geim: '*Graphene opened up a material world we didn't even know existed.*'

2.1 Crystal structure and electronic band structure

The existence of a single sheet of atoms was not considered probably due to the atom's thermodynamic instability [51], until the present century, when scientists managed to peel off a 2D monolayer of carbon atoms from bulk graphite [10, 11]. Fig. 2.1(a) shows the sheet composed in a tightly bonded honeycomb-like hexagonal structure of carbon atoms also called 'graphene' [52]. Carbon is a material in Group-IV of the periodic table and has four valence electrons in its outermost shell. Carbon atoms have the tendency to form three symmetrical covalent bonds because the $2s$, $2p_x$ and $2p_y$ orbitals can be transformed into three symmetric sp^2 hybrid orbitals with planar symmetry as shown in Fig. 2.1 (b). Notice that the p_z orbital remains unhybridised. These sp^2-hybridised carbon atoms with triangular planar structure form σ-bonding with the neighbouring carbon atoms and replicate the process to form a 2D crystal structure, earlier defined as a graphene sheet. The distance to the

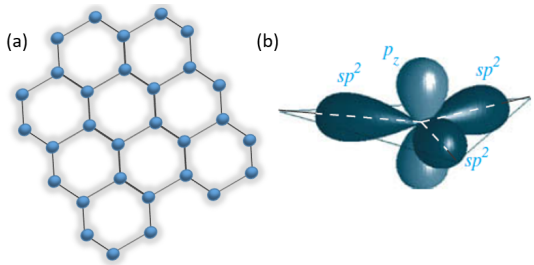


Figure 2.1: (a) The graphene crystal structure. (b) The symmetrical covalent bonding of carbon atoms and the tetrahedral symmetry of sp^3 hybrid orbital [53].

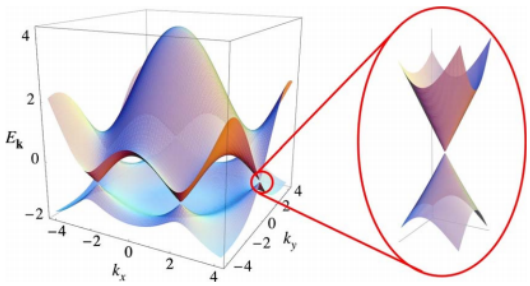


Figure 2.2: Electronic dispersion in the honeycomb graphene lattice calculated using tight-binding approximation. The conductance band touches the valence band at the points named Dirac points [54].

nearest neighbouring carbon atom is 0.142 nm. The graphene sheet shows strong mechanical strength and very high electrical conductivity. Now the question is: Where does this mechanical strength and electrical conductivity come from? The strong σ-bondings in the planar structure provide the mechanical strength to the material, and the excellent electrical conductivity originates from the unhybridised p_z orbital, which forms much weaker π-bonding with its neighbouring atoms. Below, we are focussing on the electronic transport properties of graphene.

2.1.1 Graphene electronic band structure

To understand the electronic transport properties of graphene, it is important to understand its electronic band structure. Theoretically, the concept of graphene electronic band structure was studied a long time ago in order to explain the properties of graphite. A simplified energy-momentum relation using theoretical argument, the tight-binding approximation for graphene lattice is described by assuming that the electrons can jump to the three nearest neighbouring atoms as [54]

$$E(k)^{\pm} = \pm\alpha\sqrt{1 + 4\cos\frac{\sqrt{3}a}{2}k_x\cos\frac{a}{2}k_y + 4\cos^2\frac{a}{2}k_y}. \tag{2.1}$$

Here, α is a fitting parameter and k is the wave vector. The $(+)$ and the $(-)$ signs correspond to the conduction and valence bands, respectively. The band structure calculated using eq.(2.1) is shown in Fig. 2.2. The conduction

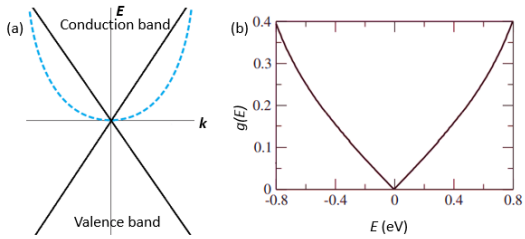


Figure 2.3: (a) Energy dispersion relation in conventional semiconductors (dashed line) and in graphene (solid line) close to the Dirac point. (b) The graphene density of state close to the Dirac point [54].

and valence bands touch at the conjugate K-points called the Dirac points. The Dirac points, also known as the charge neutrality points, express a key feature of graphene, i.e. zero-bandgap nature of monolayer graphene. The zero bandgap nature of graphene in the context of graphene transistor is a very important phenomenon and is the key to understanding the electrical characteristics of graphene transistors. In conventional semiconductors, the energy and momentum relation involves reduced mass of the free carriers and can be expressed as:

$$E(k) = \frac{\hbar^2 k^2}{2m^*}.$$

Here, $\hbar$ is the Planck's constant, k is a wave vector and m^* is the effective mass of the charge carrier. Both electrons and holes experience different effective mass in a semiconductor, which result in different total energy; thus, holes and electrons behave differently. Zooming in close to the Dirac point in Fig. 2.2 reveals the highly symmetrical nature of the dispersion relation in the vicinity of the Dirac point. According to the tight-binding approximation, the graphene quasi particles exhibit a linear energy dispersion relation. A linear conical dispersion relation in the vicinity of the Dirac point is described in terms of the Fermi velocity (v_F) as:

$$E(k) = \pm \hbar v_F \sqrt{k_x^2 + k_y^2}. \tag{2.2}$$

Fig. 2.3 shows the parabolic relation of E versus k for common semiconductors in comparison with graphene shown by the linear curve. The linear dispersion relation indicates a massless nature of graphene charge carriers. Normally, massless particles like fermions governed by the Dirac equation are described by the Fermi velocity instead of the velocity of light. This means that both electrons and holes in graphene exhibit a constant Fermi velocity $v_{\mathrm{F}} = 10^6$ m/s, irrespective in momentum, which indicates the origin of superior carrier transport properties of graphene. It further shows that, theoretically, the transport properties of electrons and holes are the same in graphene.

2.1.2 Graphene density of states and carrier concentration

The density of states is another important aspect of the electronic band structure since it defines the carrier concentration. The density of states (number of

states per unit energy interval) in graphene close to the Dirac point is derived from the momentum energy relation as:

$$g(E) = \frac{2|E|}{\pi(\hbar v_f^2)}. \tag{2.3}$$

The density of states is zero at zero Fermi energy. Zero density of states makes graphene a semiconductor-like material, while zero-bandgap attributes' resemblance to graphene is a semi-metal-like material. The density of states derived from eq. (2.3) is shown in Fig. 2.3(b). It can be seen that the density of states increases as the Fermi energy level moves away from the charge neutrality point.

The charge carrier concentration is defined by the carrier distribution in the valence or conduction band and is given by the density of state (g) times the probability (f) that a state is occupied or empty:

$$n = g(E) \cdot f_f(E). \tag{2.4}$$

Here $f_{\mathrm{f}}(E)$ is the Fermi-Dirac probability function. The carrier concentration for the volume of a given system is obtained by taking the integral of eq. (2.4). Solving the integral of the above equation gives a simple analytical expression relating the charge carrier concentration in graphene directly to the Fermi level:

$$n = \frac{g}{4 \cdot \pi} \left(\frac{E_f}{\hbar v_f} \right)^2. \tag{2.5}$$

The position of the Fermi energy (E_{f}) level is determined by the carrier type and the density in the graphene sheet. In conventional semiconductors, according to energy band theory, when the Fermi energy level lies at the midgap, the semiconductor is called the intrinsic semiconductor. In the p-doped semiconductor, the E_{f} moves closer to valence band, and in the n-doped semiconductor, the E_{f} moves closer to the conduction band. Quite similar but in monolayer graphene where bandgap does not exist, we see the Fermi energy level movement with reference to the Dirac point. So in cases when E_{f} is higher than the Dirac point and lie within the conduction band, the graphene is n-doped, and when E_{f} is below the Dirac point into the valence band region, the graphene is p-doped. Fig. 2.4 shows the simplified illustration of the above mentioned two situation when the E_{f} is in the valence band and in the conduction band.

2.1.3 Intrinsic and extrinsic carrier concentration

At this stage, it is important to distinguish between intrinsic and extrinsic graphene properties. Graphene can be defined as being of intrinsic nature, when the Fermi energy level lies exactly at the Dirac point, which means that there is no external doping. In such a system, at T = 0 K the conduction band is completely empty and the valence band is completely filled, and the Fermi level lies at the Dirac point [55]. With this definition in mind, the graphene used in all practical applications is extrinsic in nature. At temperature T > 0, there are thermally generated carriers present at all times in the system. The

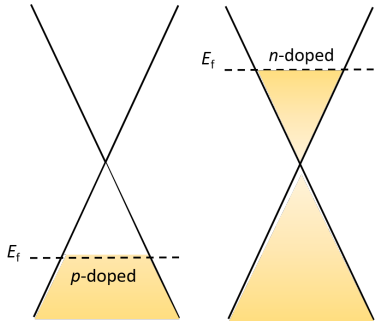


Figure 2.4: Simplified illustration of Fermi energy level in p-doped and n-doped graphene.

temperature dependent thermally generated carrier density is given by [56]:

$$n_{th} = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_f}\right)^2 \tag{2.6}$$

where k_B is the Boltzman constant. In the absence of external doping, one can say that n_{th} is the intrinsic carrier concentration of graphene at a given temperature. When the graphene is transferred onto a foreign substrate, usually the charged impurities at the interface or in the substrate oxide induce the so-called residual charge carrier concentration (n_i) in the graphene. Considering graphene in a transistor configuration, where it acts as the transistor channel, one can make graphene extrinsic via doping by applying positive or negative gate voltage. The net charge carrier concentration in the extrinsic graphene is given as:

$$n = \sqrt{n_0^2 + (C_{ox} \cdot (V_G - V_{Dir})/q)^2} \tag{2.7}$$

Here, $n_0 = \sqrt{n_{\mathrm{i}}^2 + n_{\mathrm{th}}^2}$ is minimum carrier density, C_{ox} is gate oxide capacitance per unit area, V_{G} is the gate voltage and q is the elementary charge.

2.2 Carrier transport in graphene and material imperfections

The high-frequency performance of graphene transistors depends on the charge carrier transport properties of graphene. The charge carrier transport occurs in the graphene sheet under the influence of an external electric field and is characterised by the low-field mobility and high-field carrier velocity.

2.2.1 Low-field mobility and high-field charge carrier velocity

The way the charge carrier responds to the electrical field is characterised by the low-field mobility and the high-field charge carrier velocity. Charge carrier mobility is an important material parameter at the lower field and is fundamental in describing the electrical conductivity, the resistivity and velocity of the charge carrier in that material. The mobility in this work is, typically,

Table 2.1: Comparison of graphene mobility with other 2D materials and semiconductors.

	Si	InAs	GaN	GaAs	MOS_2	BP	graphene
Mobility($10^3 cm^2/Vs$)	1.4	33	1.6	8	0.2 [58]	1 [59]	100 [13]
E_g(eV)	1.12	0.36	3.4	1.43	1.8	2	0

extracted from the transfer characteristic of the GFET or from the output characteristics at a low electric field. As mentioned above, graphene possess high intrinsic carrier mobility. Table 6.1 shows the mobility of the graphene in comparison with other 2D materials and conventional semiconductors at room temperature. However, the RF transistors operate at very high electric field, where the charge carrier velocity is considered to be the more appropriate parameter. In particular, the intrinsic transit frequency of a FET device is defined by the velocity as $f_T \approx v_d/(2\pi L)$, where v_d is the charge carrier velocity and L is the gate length. Charge carrier drift velocity under the applied electric field is modelled by [57]:

$$v_d = \frac{\mu_{eff} E_{int}}{(1 + (\frac{\mu_{eff} E_{int}}{v_{sat}})^\beta)^{1/\beta}}. \tag{2.8}$$

Here, μ_{eff} is the effective low-field mobility, v_{sat} is the saturation velocity, β is a fitting parameter and E_{int} is the intrinsic electric field along the channel. From eq. (2.8), it can be seen that the velocity is directly proportional to the electric field. With increasing the electric filed the velocity of the charge carriers increases and continue to increase until it becomes insensitive to further increase in the applied field and becomes saturated, approaching the value called 'saturation velocity'. The charge carrier velocity in the FETs channel can be evaluated from the drain current and also from the RF transit frequency f_T by using the delay time analysis. These methods will be considered in detail in the next chapters. Saturation velocity can also be evaluated theoretically by using the model which assumes that v_{sat} is limited by inelastic emission of optical phonons [44, 56]:

$$v_{sat} = \frac{2}{\pi} \frac{w_{OP}}{\sqrt{\pi n}} \sqrt{1 - \frac{w_{OP}^2}{4\pi n {v_f}^2}} \frac{1}{N_{OP} + 1}. \tag{2.9}$$

Here, $\hbar w_{\text{OP}}$ is the optical phonon energy, $N_{OP} = 1/[exp(\hbar w_{OP}/kT) + 1]$ is the phonon occupation and n is the charge carrier concentration. The above equation takes into account the temperature dependence of v_{sat} also. By assuming a negligible effect of temperature on v_{sat}, a more simple approximation of v_{sat} can be used [40]:

$$v_{sat} = \frac{2}{\pi} \frac{w_{OP}}{\sqrt{\pi n}}, \tag{2.10}$$

which indicates that for a given total carrier concentration n, the v_{sat} is defined by the optical phonon energy $\hbar w_{\text{OP}}$ of the material. The v_{sat} for graphene on SiO_2 substrate was recorded to be in the range of 1-2 $\times 10^7$ cm/s and is limited by the relatively low surface optical phonon energy $\hbar w_{\text{OP}} = 55$ meV of SiO_2 [44, 56]. In Paper [C] and [D], we systematically investigated

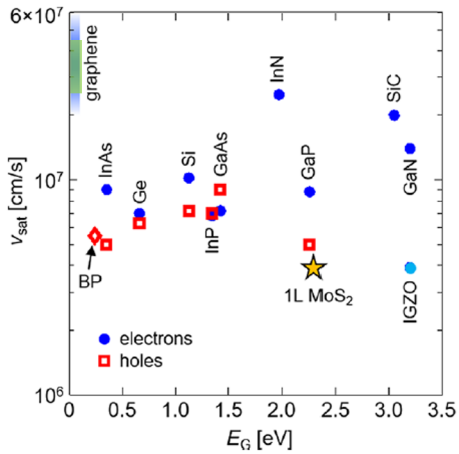


Figure 2.5: Charge carrier saturation velocity of graphene at room temperature in comparison with that of conventional semiconductors [60]. Note: The green bar overlapping the blue bar represents the velocity measured in this work by using CVD graphene on different substrate materials.

the effects of $\hbar w_{\mathrm{OP}}$ of substrate dielectrics on the v_{sat} and the GFET high-frequency performance. Fig. 2.5 shows the saturation velocity of the graphene in comparison with other 2D materials and semiconductors. It can be seen that graphene is the material with the highest v_{sat} making it graphene a promising channel material for RF electronics. The v_{sat} measured in hexagonal boron nitride (hBN) encapsulation graphene Hall bar devices is in the range of 3-6 $\times 10^7$ cm/s [15], because the hBN $\hbar w_{\mathrm{OP}}$ is more than 100 meV. As reported in Paper [D], the saturation velocity measured in the top-gated two finger GFETs on diamond, which is material with highest OP energy, can be as high as v_{sat}=3.3 $\times$ 10^7 cm/s.

2.2.2 Material imperfections

As mentioned above, graphene possesses an extremely high intrinsic mobility of charge carriers. However, graphene is atomically thin layer of atoms and is very sensitive to its surrounding materials. In practical devices, the graphene mobility drops to several fold due to the number of extrinsic factors. For instance, the very first paper studying the field-effect phenomenon in a graphene sheet was submitted by Novoselov [10] in 2004, where he reported the mobility up to 10^4 cm^2/Vs at room temperature. A few years later, Bolotin et al. reported that the carrier mobility in graphene can be as high as 10^5 cm^2/Vs at room temperature [13]. The reasons for such difference is that Novoselov et al. prepared the graphene devices on a SiO_2 substrate where the charge carrier impurities at the interface and in the oxide limit the charge carrier mobility. In contrast, the paper by Bolotin et al. reports on devices fabricated by using suspended single layer graphene. Free standing graphene preserves its high quality close to ideality and the mobility in such super clean graphene sheet is neither limited by lattice acoustic phonons scattering at high temperature nor by the impurity scattering [61–63]. However, the freestanding graphene is not viable from the device fabrication point of view. Graphene in devices is

inevitably have to be contact with foreign materials and dielectric substrates for real electronic applications. As the graphene is transferred onto a dielectric substrate, its intrinsic superior properties degrade dramatically. This is because carrier scattering rate increases many fold due to the number of different extrinsic scattering mechanisms such as remote interfacial phonon scattering, charged impurity scattering, scattering by ripples, neutral defect scattering and resonant scattering [64]. When various scattering mechanisms are involved, their relative contributions to the net mobility can be counted using Matthiessen's rule as [65]:

$$\tau^{-1} = \tau_{cl}^{-1} + \tau_{sr}^{-1} + \tau_{op}^{-1} + \tau_{LA}^{-1} + \tau_{corr}^{-1} = \sum \tau_{x}^{-1}. \tag{2.11}$$

Here, τ is the scattering time between two scattering events, and the subscript (cl) represents Coulomb scattering, i.e. by charged impurities, (sr) represents short-range scattering, i.e. scattering by neutral defect, (op) indicates remote optical phonon scattering, (LA) longitudinal acoustic phonons, and (corr) is for corrugations or graphene ripple scattering. All these scattering mechanisms contribute to mobility through the expression [66, 67]:

$$\mu = \frac{q v_F^2 \tau}{E}, \tag{2.12}$$

where E is the electric field. Coulomb scattering is the long-range scattering mechanism associated with the charged impurities at the interface and in the gate or substrate dielectrics. Long-range scattering is considered to be the main scattering mechanism controlling the carrier transport in graphene FET devices at relatively low carrier concentration [55]. Short-range scattering is also present in graphene and associated mainly with the lattice defects. It dominates at relatively high carrier concentration and in cleaner samples. Another extrinsic scattering mechanism is the remote OPs at low temperature and is inversely proportional to the carrier concentration simply because higher carriers densities lead to a higher scattering rate [61]. The other significant scattering effects can be due to the ripples in graphene and is partially related to the substrate roughness [68]. To bring graphene-based technology to a higher level, it is necessary to overcome the limitations of extrinsic scattering mechanisms.

In this context, an endeavor to reach the intrinsic graphene transport properties comes with the approach of using an exfoliated hBN layers as the substrate material. The hBN is a wide bandgap material. It has hexagonal lattice symmetry like graphene crystal and has a lattice mismatch of 2.0%. Recently, room temperature mobility well above 70×10^4 cm^2/Vs was reported for hBN encapsulated graphene Hall bar devices [14, 69], indicating that hBN is a promising dielectric material for graphene devices. However, it is not yet feasible for wafer scale device fabrication.

An inevitable feature associated with material imperfections is spatially inhomogeneous screened Coulomb potential created by charged impurities in the dielectric layers adjacent to the graphene sheet. The charged impurities are typically associated with the oxygen vacancies in the adjacent dielectrics and/or water molecules trapped at the graphene-dielectric interfaces [71, 72]. This causes a spatially inhomogeneous random network of two dimensional

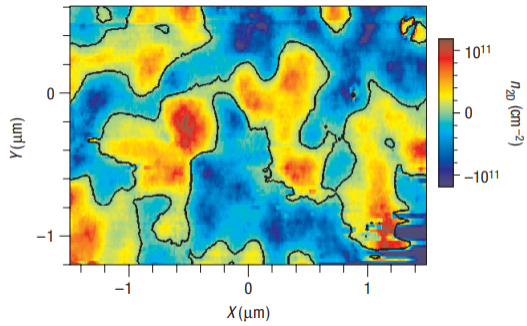


Figure 2.6: Mapping of the charge carrier density measured at the Dirac point [70].

electrons and holes puddles in the graphene sheet as shown in Fig. 2.6. These laterally inhomogeneous densities of charged impurities have been reported in many studies [62–64, 66, 73]. The inhomogeneous electron and hole puddles define the minimum conductivity, measured at the Dirac point.

The variations of the GFET performance from device to device over the chip surface, observed in this thesis work, is largely attributed to the spatially inhomogeneous material quality. We exploited this largely distributed material quality over the chip as a tool to study the effect of charge carrier transport in a channel on the high-frequency performance of GFETs in Paper [A]. Furthermore, we also take into consideration the variations in GFET performance when designing GFET IC amplifiers, as discussed in Paper [G].

Chapter 3

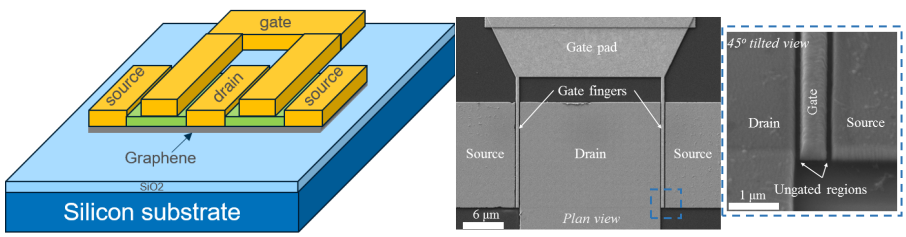
High-frequency graphene field-effect transistors

In this chapter, features of the design, fabrication and operation of the high-frequency GFETs are considered, including modeling of the charge carrier transport and high-frequency performance. General operational principles of GFET are similar to that of MOSFET, however, there are some distinguishable features associated, first of all with zero bandgap in monolayer graphene which results, in particular, the ambipolar transport in the GFET channel.

3.1 Design and fabrication of high-frequency GFETs

3.1.1 High-frequency aspects of design

In this work, the GFETs in the planar top-gate configuration and two gate fingers design were developed and optimized for the highest high-frequency performance, as shown in Fig. 3.1. The high-frequency performance of RF FETs are characterised using the FOMs, which are the transit frequency f_{T} and maximum frequency of oscillation f_{max} and can be expressed using the



(a) (b)

Figure 3.1: (a) A schematic cross-section view of the GFET. (b) SEM of a two fingers GFET with two source, a drain and gate electrodes. Magnified planar and 45° tilted view of the gate area in (b) corresponding to the dashed line box.

small-signal equivalent circuit model as [74]:

$$f_T = \frac{f_{T-int}}{1 + g_{ds}R_C + \frac{C_{gd}\cdot g_m \cdot R_C}{C_{gs}+C_{gd}} + \frac{C_{GP}}{C_{gs}+C_{gd}}}, \tag{3.1}$$

$$f_{\max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}\left(R_i + \frac{R_C}{2} + R_G\right) + g_m R_G \frac{C_{gd}}{C_{gs}}}}, \tag{3.2}$$

where, g_{m} is the transconductance and g_{ds} is the drain conductance. R_{C} is the contact resistance, R_{i} is the charging resistance of the gate-source capacitance and R_{G} is the gate resistance. The C_{gs} and C_{ds} are the gate-source and gate-drain capacitances, and C_{GP} is the gate-pad capacitance. The $f_{\mathrm{T-int}} = g_{\mathrm{m}}/2\pi(C_{\mathrm{gs}} + C_{\mathrm{gd}})$ is the intrinsic transit frequency. To achieve high FOMs, the GFETs are designed taking into account the following considerations and conditions.

• The intrinsic f_{T} and $f_{\max}$ can be expressed via gate length as [75]:

$$f_{T-int} = \frac{1}{2\pi\tau_{int}} = \frac{v_d}{2\pi L}, \tag{3.3}$$

$$f_{max-int} \approx \frac{f_{T-int}}{\sqrt{R_i g_{ds}}}, \tag{3.4}$$

where τ_{int} is the intrinsic transit time, i.e. the time of drift of charge carriers between source and drain. It can be seen from eqs. (3.1) and (3.2), that for highest f_{T} and $f_{\max}$ the gate length should be as short as possible. On the other hand, at relatively short gate length, the contact resistance associated with ungated regions starts to limit the high-frequency performance. In the current design/technology optimal L is approx. 0.5 μm.

• Analysis indicates that, relatively large gate width and two gate fingers should be used to minimise the effects of the pad capacitances. It follows from a simplified expression for the time delay in the GFET as: [75]

$$\tau = \frac{1}{2\pi f_T} = \tau_{int} + \tau_{pad}, \tag{3.5}$$

and

$$\tau_{pad} = \frac{C_{PG}}{g_m \cdot W}$$

where τ_{pad} is the delay associated with discharging of the gate pad capacitance. As it can be seen that the effect of τ_{pad} can be reduced by increasing the gate width. Current optimal design / technology utilises the two gate fingers with total W=30 μm as shown in Fig. 3.1 (b).

• Consideration of eqs. (3.1) and (3.2) indicates that the ungated regions should be as short as possible to minimise the effect of total contact resistance as shown in zoom Fig. 3.1 (b). With current technology the ungated region length L_{acc}=100 nm, which is the lower limit defined by the e-beam lithography in this fabrication process flow. To get rid of the access area and related resistance, in the future generation of GFETs the self-aligned gate technology can be pursued.

• The top-gate configuration is used with the aim to minimise the parasitic

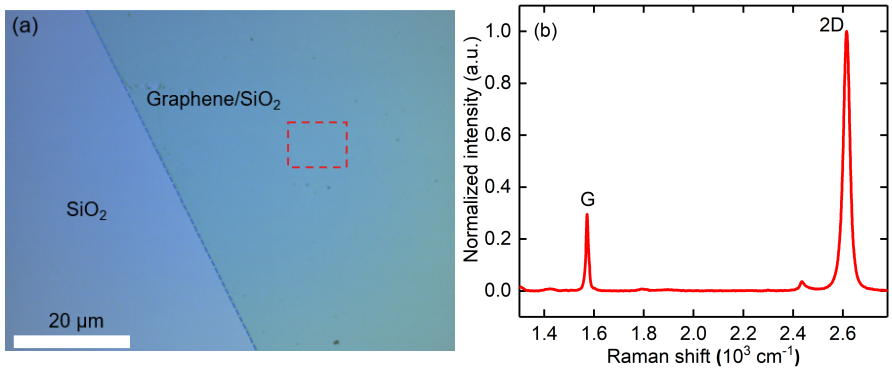


Figure 3.2: (a) Optical micrograph of the monolayer graphene transferred on Si/SiO_2. (b) The Raman spectrum taken at marked dashed box in (a).

gate-source and gate-drain capacitances.

• In the planar gate technology, rather thick gate electrode of 0.3 μm Ti/Au is used to minimise the limiting effect of the R_G on extrinsic f_{max} as follows from eq. (3.2).

3.1.2 CVD graphene selected for high-frequency GFETs

The GFETs with state-of-the-art high-frequency performance demonstrated so far utilise graphene fabricated by using three basic technologies: i) mechanical exfoliation, ii) epitaxial growth on SiC substrates and iii) chemical vapour deposition (CVD) [24,27,30,34,48,76]. The mechanical exfoliation from graphite inherently provides the highest quality graphene, because of the fewer defects, less impurity residuals and no grain boundaries. The exfoliated graphene demonstrates room temperature mobility over $1 \cdot 10^5$ cm^2/Vs and saturation velocity up to $6 \cdot 10^7$ cm/s [13, 15, 69]. However, the exfoliated graphene flakes are limited in size of typically few tens μm^2, and the technology is not compatible with the standard high-volume, large-scale CMOS processes. The epitaxial graphene can be obtained on the large area SiC substrates and with rather high quality [77, 78]. However, the drawback of this technique is the limited possibility of integration on the common grade semiconductor substrates. The CVD graphene can be grown on large areas and transferred onto arbitrary substrates. From this point of view, the CVD graphene is the technology of choice for the development of high performance high-frequency electronics based on GFETs. Recent advances in the CVD technology allowed for fabrication of graphene with mobility comparable to that of the exfoliated graphene encapsulated by hBN [14]. The CVD graphene is typically grown on a Cu foil, acting as a catalyst, using precursors gas flows. In the next step, graphene is transferred onto a substrate for subsequent device processing [79]. The GFETs and devices developed in this work were fabricated using CVD graphene with low-field mobility up to 2500 cm^2/Vs. The CVD graphene used in Papers [A] to [C] were grown and transferred onto SiO_2/Si substrates by AMO and Aachen University. Graphene used in Papers [D] to [G] is supplied by Graphenea and transferred using the 'easy transfer' method developed by

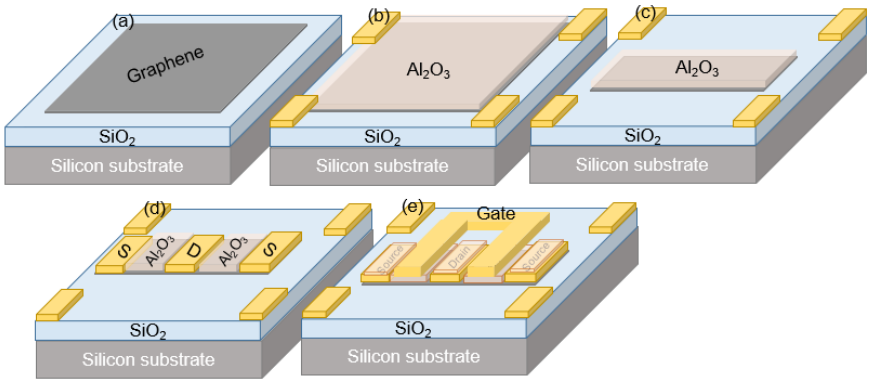


Figure 3.3: Schematic of the fabrication steps of two fingers top-gate GFET.

the company. The monolayer graphene was used due to its superior electron transport properties, better than that of the bilayer or multilayers graphene. Fig. 3.2(a) shows the optical micrograph of a CVD graphene transferred onto a SiO_2/Si substrate. Fig. 3.2(b) shows the Raman spectrum taken from the region marked by the dashed line in Fig. 3.2(a).

3.1.3 Fabrication development

The fabrication process, developed for GFETs reported in Papers [A]-[C], [E] and [G], starts with transfer of the graphene onto a high-resistive Si substrate covered by 1 μm thick SiO_2 layer grown by wet oxidation, as shown in Fig. 3.3(a). Relatively thicker SiO_2 was used with the aim to reduce the parasitic pad capacitances in the GFETs. A modified fabrication process was adopted for the GFET fabrication with an aim to preserve the graphene from contamination during fabrication. As a first step, the graphene sheet was covered with a dielectric layer as shown in Fig. 3.3(b), in Paper [A] to [G] it was Al_2O_3 and in Paper [E] it was Ti/TiO_2. This modification, in comparison with previously used process, serves two important purposes:
• It provides a cleaner metal-graphene interface under the contact electrode.
• It provides a cleaner interface between the top-gate dielectric and graphene channel.

In contrast, the previously used GFET fabrication process started with the formation of source and drain contacts and thus does not protect the graphene channel from contamination by residues of e-beam resists, adsorbent molecules and other processing chemicals [63, 72, 80]. The next step of the modified fabrication process was defining the mesa structure, as shown in Fig. 3.3(c). Ohmic contacts were formed by patterning the contact area using e-beam lithography, followed by etching the protective oxide layer by buffer oxide etchant (BOE) and finally depositing Ti/Pd/Au (1 nm/15 nm/250 nm) metal layers, see Fig. 3.3(d). It has been found via Raman spectra analysis that etching the oxide layer with BOE allows for the effective removal of polymer residues from the graphene surface. More details are given in the next sections. The next processing step was the deposition of a second layer of Al_2O_3 gate

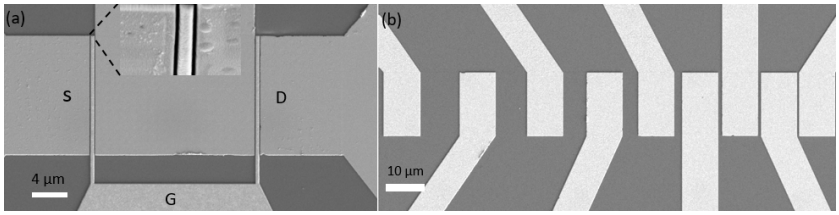


Figure 3.4: SEM micrographs of (a) two finger top-gate GFET (b) TLM test structure.

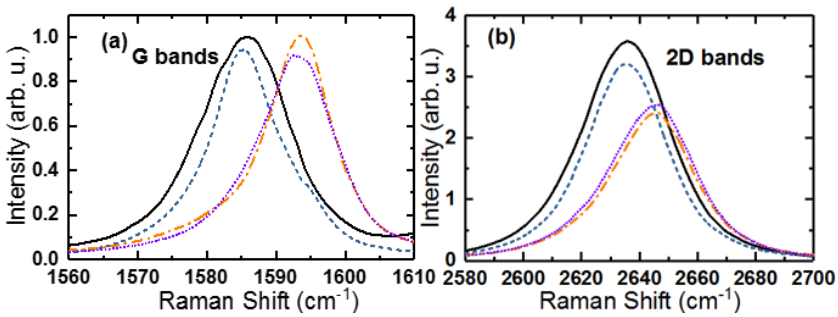


Figure 3.5: Raman spectra of the G bands (a) and 2D bands (b) of graphene as transferred (solid line) and after patterning with Al_2O_3 using MMA-EL6 (dashed line), without Al_2O_3 using PMMA (dashed dotted line), and without Al_2O_3 using MMA-EL6 (dotted line).

dielectric using an atomic layer deposition technique, where the first few Al layers were deposited by e-beam evaporation and then thermally oxidized served as a seed layer. Next, gate fingers were patterned, and a metal stack of Ti/Au (10 nm/270 nm) was deposited, Fig. 3.3(e). The final processing step was the formation of contact pads for microprobes. All processing steps were carried out using e-beam lithography and e-beam evaporation. Typical SEM micrographs of top-gated double gate finger GFET and transfer length method (TLM) test structures are shown in Fig. 3.4.

Control removal of polymer residue

Raman spectroscopy was used for monitoring the graphene quality in response to development/modification of fabrication technology. In particular, analysis of the Raman spectra in Fig. 3.5 allows for evaluation of the doping effect caused by resist residues and verifying the effective removal of polymer residues in the modified fabrication technique. To verify the effective removal of e-beam resist residues in the modified fabrication method, the following test samples were prepared on Si/SiO_2 substrates and analysed using Raman spectroscopy:
i) graphene with Al_2O_3 layer after developing the MMA-EL6 e-beam resist followed by patterning the Al_2O_3 layer, which represents the modified technology;
ii) graphene without Al_2O_3 layer after developing by MMA-EL6 and PMMA e-beam resists, which represents the previously used technology [24, 25];
iii) as-transferred graphene used as a reference.

As can be seen in Fig. 3.5, the positions and intensities of the G and 2D peaks corresponding to patterning with Al_2O_3 using MMA-EL6 match

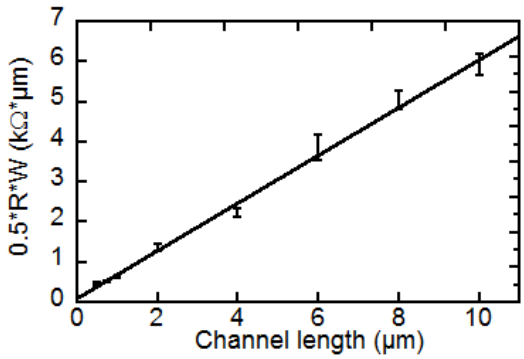


Figure 3.6: The $0.5 \times R \times W$ of a TLM tests structure versus channel length.

closely to those of the as-transferred graphene. The positions of the peaks corresponding to patterning without Al_2O_3, using both MMA-EL6 and PMMA are upshifted, and the intensities of the 2D peaks are reduced. It was shown that the positions of the G and 2D peaks are defined by concentration of charge carriers and strain [81, 82]. The 2D to G peak intensity ratio, I(2D)/I(G), is a strong function of the charge carrier concentration and does not depend on the strain [81–83]. The downshifts of the G and 2D bands positions, reported in [84] for PMMA-covered graphene, are not accompanied by remarkable changes in the I(2D)/I(G) ratio and, hence, are explained by the tensile strain produced by PMMA. The upshifts and decrease in the I(2D)/I(G) ratio caused by removing polymer residues via post-annealing, reported in [85, 86], are explained by formation of charged defects resulting in hole doping. Our analysis indicates that the upshifts and the I(2D)/I(G) reduction observed in our experiments corresponding to patterning without Al_2O_3, using both MMA-EL6 and PMMA (see Fig. 3.5) can only be explained by hole doping [81], apparently caused by residues of polymers. The matching of positions and intensities of the G and 2D peaks corresponding to patterning with Al_2O_3 using MMA-EL6 confirms that, in the case of the modified technique, the polymer residues are effectively removed.

3.1.4 Low resistive graphene-metal junctions

Realisation of low resistive metal-graphene junctions is a challenging task for researchers working with graphene device technology. There are basically two methods of contact formation in GFET technology: (i) the conventional top or planar type contacts and (ii) the side or edge type contacts [49]. In this study, planar contacts with very low specific width contact resistivity ρ_C down to 90 $\Omega \times \mu$m have been demonstrated. For contact resistance measurements, multi-terminals technique of the TLM was implemented [87, 88]. The TLM is the most commonly applied method to extract the contact resistance, in particular, because it takes into account the edge effect and current crowding [89, 90]. The parameter characterising the metal-graphene contact is the specific width contact resistivity $\rho_C = R_C \times$ W [91]. A TLM test structure is shown in Fig. 3.2(b). In TLM methods, a chain of identical contacts are fabricated with different channel lengths between them. The total resistance R between

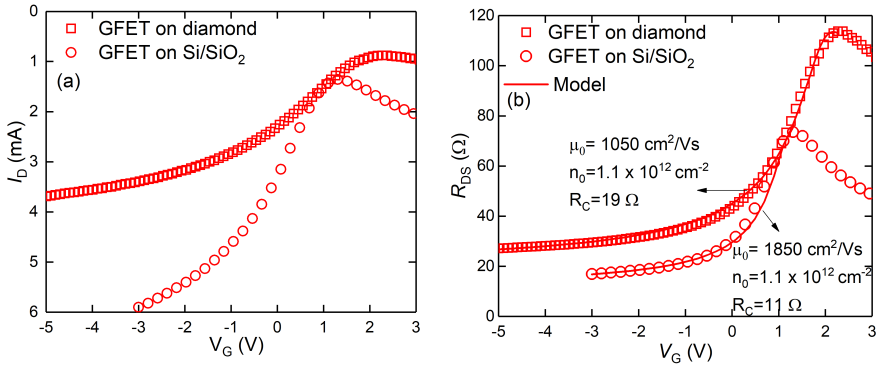


Figure 3.7: Typical transfer characteristics (a) and corresponding dependences of the drain resistance (R_{DS}) on the gate voltage (V_{G}) (b) of the GFETs on diamond and Si/SiO_2 substrates. The solid lines represent fitting by the drain resistance model using eqs. (3.8).

the contacts is measured by using DC IV characterisation. The R measured between the two contacts is a combination of contact resistance R_{C}, and the graphene sheet resistance R_{sh} and can be expressed as:

$$R = 2R_C + \frac{R_{sh}L}{W}. \tag{3.6}$$

Where L is the graphene channel length and W is the channel width. The total measured R multiplied by 0.5W for different channel spacings are then plotted versus L as shown in Fig. 3.6. The slope gives the sheet resistance of the graphene while R_{C} is obtained from y-intercept at L = 0. The measured ρ_{C} in this way is 90 $\Omega \times \mu$m, which is lower than the edge type contacts and is close to the theoretical limit of 88 $\Omega \times \mu$m [92].

3.2 DC performance and models of GFETs

3.2.1 Transfer characteristics and drain resistance model

Typical transfer characteristics of GFETs on diamond and Si/SiO_2 substrates and corresponding dependences of the drain resistance on gate voltage are shown in Fig. 3.7. The dependences reveal characteristic minimum conductivity at Dirac voltage manifesting the graphene's ambipolarity. The minimum conductivity is defined mainly by the impurities in the system as in [63, 73]:

$$\sigma_{min} = \mu_0 n_0 q \tag{3.7}$$

where μ_0 is the low-field mobility and n_0 is the residual carrier concentration defined by the spatially inhomogeneous screened Coulomb potential by neglecting the concentration of the thermally generated carriers [73]. The n_0 can be found using the random phase approximation formalism [73]. Alternatively, n_0 and μ_0 can be evaluated via fitting the drain resistance model [93]:

$$R_{DS} = R_C + \frac{L}{qW\mu_0 n} \tag{3.8}$$

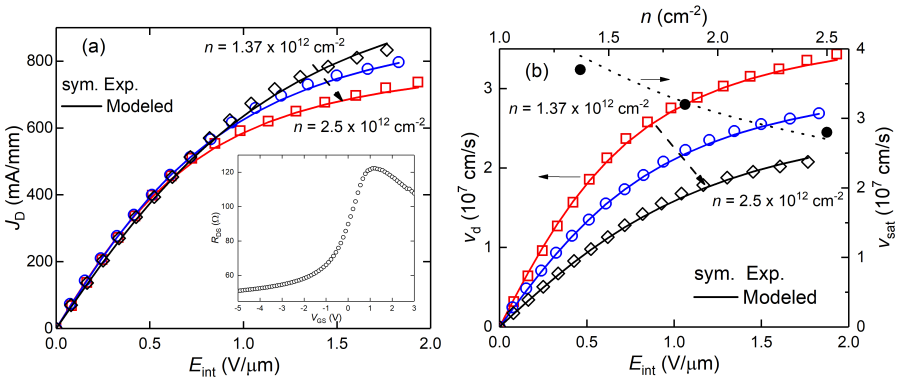


Figure 3.8: Saturation of the drift velocity (a) Drain current density (J_D) vs. intrinsic drain field (E_{int}) of the GFET on diamond substrate with 0.75 μm gate length at different gate voltages of V_G=1, 0.5, 0 V increasing in the arrow's direction. Shown are also corresponding total concentrations of the charge carriers. Inset shows the drain resistance dependence on the gate voltage. The lines represent the drain current density modelled using eqs. (2.8), (3.9) and (3.10). (b) The effective drift velocity of the charge carriers (v_d) vs. intrinsic drain field calculated from dependences shown in (a) using eqs. (3.9), (3.10). The solid lines represent the drift velocity calculated using the drift velocity model, eq. (2.8). The dashed line represents the saturation velocity dependence on concentration calculated using the saturation velocity model, eq. (2.10).

where R_C is the total source and drain series resistance including a graphene-metal junction resistance and resistance associated with ungated regions of the channel, n is the total carrier concentration as defined in eq. (2.7), L is the gate length, W is the gate width and n is the total carrier concentrations, C_{ox} is the gate capacitance per unit area. Fig. 3.7 shows the R_{DS} vs. V_G of the GFETs together with fitting curves of the model and corresponding values of the μ_0, n_0 and R_C found as fitting parameters.

3.2.2 Output characteristics, drain current and drift velocity models

Fig. 3.8(a) shows the drain current densisty (J_D) versus intrinsic drain field (E_{int}) of a GFET on diamond substrate with 0.75 μm gate length at different gate voltages of V_G=1, 0.5, 0 V increasing in the arrow's direction. Shown are also corresponding total concentrations of the charge carriers. The drain current density and intrinsic drain field are calculated as J_D=I_D/W and $E_{int} = (V_D - I_D R_C)/L$. The drain current density can be expressed as:

$$J_D = q n_{eff} \mu_{eff} E_{int} = q n_{eff} v_d \tag{3.9}$$

where v_d is the effective drift velocity of the charge carriers and n_{eff} is the effective carrier concentration by taking into account of the effects of depletion at the drain side and thermal generation of carriers due to self-heating at relatively high drain fields. The n_{eff} can be expressed as [15]:

$$n_{eff} = \sqrt{n_0^2 + (C_{ox}/q(V_G - V_{Dir} + V_d/2))^2} \tag{3.10}$$

where V_G, V_{Dir} and V_d are intrinsic gate, Dirac and drain voltages, respectively. The n_0 is the residual carrier concentration at elevated temperature caused by

self-heating and calculated as: $n_0 = \sqrt{n_i^2 + n_{th}^2}$ [56]. The n_i can be found using the drain resistance model and n_{th} calculated using the thermal resistance model [56]. The effective drift velocity v_d can be obtained using eq. (2.8). The μ_{eff} can be found from the output characteristics as $\mu_{eff} = g_{ds}L/neW$ [90]. The lines in Fig. 3.8(a) represent the drain current density modelled using eqs. (2.8), (3.9) and (3.10). Fig. 3.8(b) shows the drift velocity calculated using the measured current density shown in Fig. 3.8(a) and eqs. (3.9) and (3.10). The solid lines represent the drift velocity calculated using the drift velocity model given by eq. (2.8) with v_{sat} as a fitting parameter. The v_{sat} is shown in Fig. 3.8(b) versus carrier concentration for the corresponding three different gate voltages. The dashed line represents the saturation velocity dependence on concentration, calculated using eq. (2.10) [15, 56]. As it can be seen, there are good agreements between the experimental measurements and the simulations in all dependences in Fig. 3.8(a) and Fig. 3.8(b).

3.3 Mobility degradation

Mobility modelling including appropriate low-field mobility and saturation velocity models are of utmost importance for characterising GFETs and for predicting their performance in circuit applications. Several GFET IV-models pay attention to velocity saturation effects at high electric fields, but low-field mobility degradation at high carrier concentrations is neglected in most models despite being observed already in early work. In Paper [F] a GFET low-field mobility model was proposed that includes mobility degradation due to an increasing number of charge carriers induced by the gate voltage. By using this mobility model, one can show that series resistance values extracted by using widely accepted resistance models overestimate the real series resistance because of the effects of mobility degradation. An effort were made to separate the two effects by examining the gate length dependence of the resistance values extracted from measurements on a set of GFETs of different gate length. A detail mathematical expression and discussion is given in Paper [F].

3.4 High-frequency performance and models of GFETs

In this section, small-signal equivalent circuit model, DC, S-parameter measurements and high-frequency performance benchmarking of GFETs are considered. The details of measurements and evaluation of the high-frequency performance of GFETs including those with record high f_T and f_{max} of 34 GHz and 37 GHz, respectively, are published in Paper [B].

3.4.1 Small-signal equivalent circuit model

In this work, the small-signal equivalent circuit of a GFET, shown in Fig. 3.9, is used for device modelling, optimisation and predicting the GFET performance and limitations. The elements within the dashed rectangle constitute the intrinsic transistor, i.e., the gate region of the transistor and the channel below. The extrinsic part of the transistor consists of the parasitic elements. The

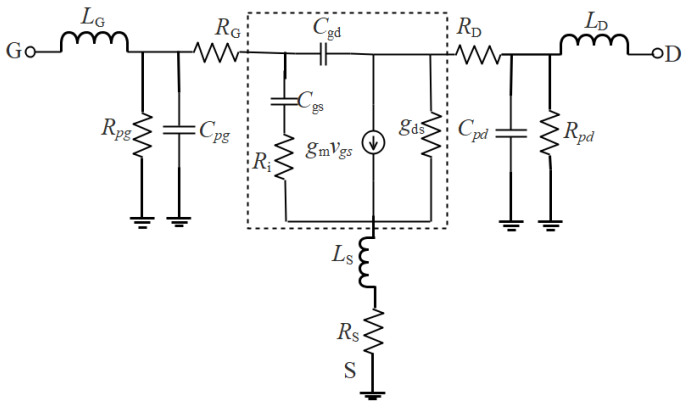


Figure 3.9: The small-signal equivalent circuit of GFET with dashed line box separating the intrinsic transistor circuit.

entire circuit consists of the following elements: intrinsic transconductance (g_m) and drain conductance (g_d); gate-source C_gs, gate-drain C_gd, drain-source C_ds; parasitic gate pad C_pg and drain pad C_pd capacitances with corresponding resistances R_pg and R_pd; gate resistance R_G; source R_S and drain R_D series resistances; charging resistance of the gate-source capacitance (R_i); inductances associated with the gate (L_G), source (L_S) and drain (L_D) leading electrodes. The equivalent circuit has been used to interpret and predict the high frequency performance of GFETs in Paper [B]. Below, a novel method of analysis of correlation between material quality and high-frequency performance of GFETs is presented.

3.4.2 Modelling of the f_T and f_max

The two main FOMs of RF transistors are f_T and f_max, which characterise the transistor's current gain and unilateral power gain, respectively [94]. The gains of the transistor can be deduced from the equivalent circuit applying Kirchhoff's laws and the rules of two-port theory allowing for deduction of the y parameters and, finally, expressions for the f_T and f_max [29]. The characteristic frequencies of the intrinsic transistor can be expressed as:

$$f_{T-int} = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)}, \tag{3.11}$$

$$f_{\mathrm{max-int}} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}R_i}}, \tag{3.12}$$

and commonly used approximations for the corresponding extrinsic frequencies of the whole transistor are [29, 95, 96],

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \frac{1}{1+g_{ds}R_C+\frac{C_{gd}\cdot g_m\cdot R_C}{C_{gs}+C_{gd}}}, \tag{3.13}$$

$$f_\mathrm{max} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}\left(R_i+\frac{R_C}{2}+R_G\right)+g_m R_G\frac{C_{gd}}{C_{gs}}}}, \tag{3.14}$$

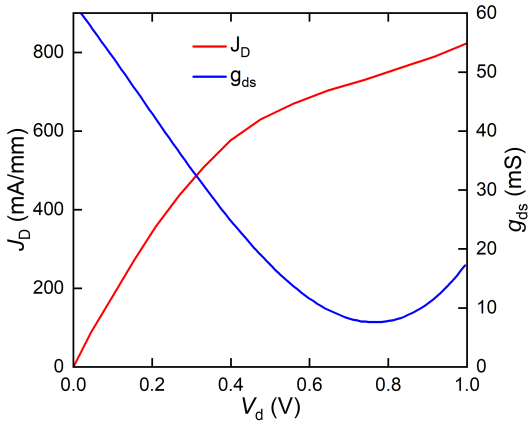


Figure 3.10: Drain current density and drain conductance versus intrinsic drain voltage.

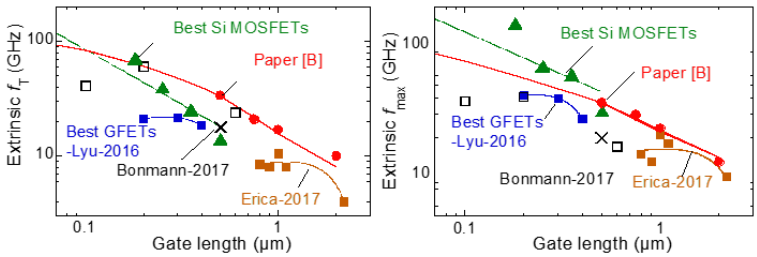


Figure 3.11: Extrinsic transit frequency (f_{T}) and (c) maximum frequency of oscillation (f_{max}) versus gate length of GFETs reported in Paper [B] (solid circles and line) shown together with previously published highest values of GFETs (squares) and Si MOSFETs (triangles).

In this paper, a methodology for extraction of the parameters g_{m}, g_{ds} and R_{C} from the DC characteristics of the GFET is proposed and considered. The capacitances can be calculated as C_{gs}=$WLC_{\mathrm{ox}}/2$ and C_{gd}=kC_{gs}, where C_{ox}=$3 \cdot \mathrm{fF} \cdot \mu\mathrm{m}^{-2}$, is the gate oxide capacitance per unit area, W is the gate width and k is the fitting parameter taking into account the decrease in charge carrier concentration at the drain side [40]. The resistances can be calculated as R_{S}=$R_{\mathrm{C}}/2$, where R_{C} is total series resistance, R_{i}=$1/(3g_{\mathrm{m}})$, $R_{\mathrm{G}} = R_{\mathrm{sh}}W/3L$ and $R_{\mathrm{sh}} = 0.08\Omega$ is the gate electrode sheet resistance [42, 74]. We assume that at low fields the Coulomb scattering dominates [66, 73]. This allows for finding the R_{C}, low-field mobility and residual carrier concentration as parameters via fitting the GFET transfer characteristics by the semi-empirical drain resistance model, eq. (3.8). The g_{ds} can be readily found from the GFET output characteristics. As an example, Fig. 3.10 shows the drain current density versus intrinsic drain voltage of a GFET on the Si/SiO_2 substrate with L=0.5 μm and W=30 μm. Shown also is corresponding drain conductivity, defined as $g_{\mathrm{ds}} = \partial I_{\mathrm{D}}/\partial V_{\mathrm{d}}$. The kink in the J_{D} curve and corresponding minimum in the g_{ds} curve manifest, first the drain current saturation and then the formation of the n_0 region at the drain side and following ambipolar channel [40]. The

intrinsic transconductance can be calculated as [42, 74],

$$g_m = v_d \cdot (C_{\mathrm{gs}} + C_{\mathrm{gd}})/L \tag{3.15}$$

with the v_{d} found using the drift velocity and the saturation velocity models, eq. (2.8) and eq. (2.9). Fig. 3.11 shows f_{T} and f_{max} versus gate length of GFETs on Si/SiO_2 substrates (solid circles). Also shown are the highest published extrinsic f_{T} and f_{max} values of GFETs (squares) [27, 34–36, 97] and Si MOSFETs (triangles) [98–101] and our previous published work (open circles) [37] for comparison. Dashed lines are polynomial fitting curves. Paper [B]. The solid lines represent modelling by the method described above using eqs. (3.13)-(3.15). As it can be seen, the simulations and measurements are in very good agreement. It can be seen also, that the GFET fabricated using our optimised technology reveal f_{T} and f_{max} values higher than those of the best reported GFETs and comparable or even higher than those of Si MOSFETs [99] at similar gate lengths. Additionally, experimental and modelled data indicate promising scaling down behaviour of our GFETs.

3.4.3 Delay time analysis concept

The delay time is the frequently used method for analysing the intrinsic performance of transistors [44, 48, 75]. In this work, the delay time analysis was used to calculate the charge carrier velocity in the graphene channel of the GFET. For this purpose, one need to find the charge carrier transit time τ related to the intrinsic transit frequency, $f_{\mathrm{T-int}}=1/(2\pi\tau)$, by removing the delay associated with the parasitic capacitances and resistances. A relationship between the $f_{\mathrm{T-int}}$ and the as measured transit frequency f_{T} can be found from the analysis of the GFET small-signal equivalent circuit pioneered by Tasker and Hughes [95], an analysis to which Nummila et al. [75] added an approximate contribution from the gate pad capacitance,

$$f_T = \frac{f_{T-int}}{1 + g_{ds}R_C + \frac{C_{gd}\cdot g_m \cdot R_C}{C_{gs}+C_{gd}} + \frac{C_{GP}}{C_{gs}+C_{gd}}}, \tag{3.16}$$

where, g_{ds}, g_{m}, C_{gs} and C_{gd} can be calculated as described in the previous section. The parasitic gate pad capacitance's C_{GP} was found to be 8 fF using the method described in [75]. From eq. (3.16), the transit time τ can easily be extracted by using:

$$\tau = \frac{\frac{1}{2\pi f_T} - \frac{1}{2}R_C(C_{gs}+C_{gd})}{1 + g_{ds}R_C + \frac{C_{pad}}{C_{gs}+C_{gd}}}, \tag{3.17}$$

From the transit time the effective charge carrier velocity in the channel can be obtained as $v = L/\tau$. This method has been applied in Paper [C] to find and compare the substrate induced charge carrier velocity in GFETs.

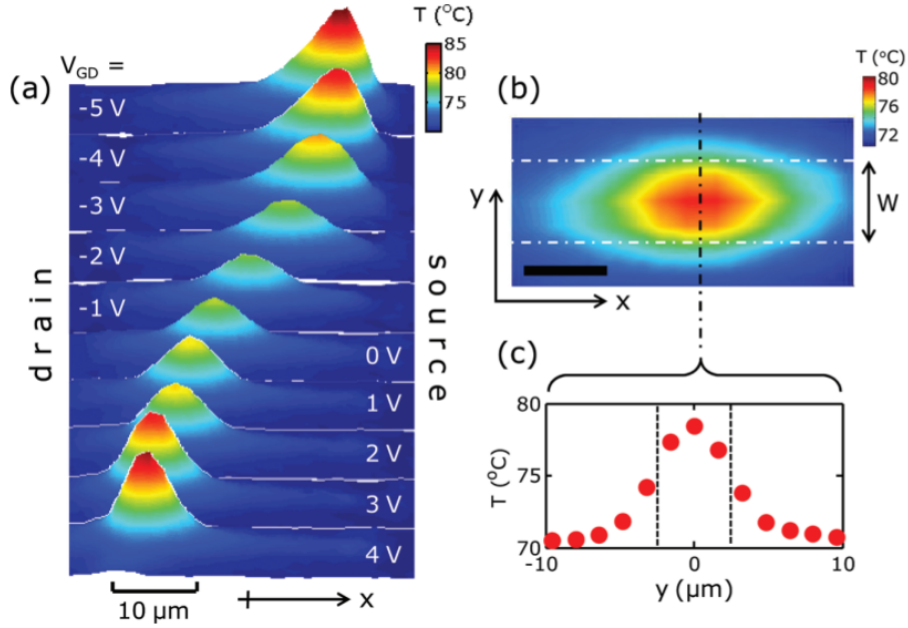


Figure 3.12: Figure taken from ref. [102] showing the temperature profile along the channel of a GFET.

3.5 Effect of self-heating on DC and high-frequency performance of GFETs

Analysis of the above models of the charge carrier transport and RF performance of the GFETs indicates that to reach the highest f_T and f_{max}, transistors should operate in the velocity saturation mode at rather high intrinsic drain fields, above approx. 1 V/μm with corresponding dissipated power density more than 1 mW/μm^2. As it is shown in [103] and Paper [E], at such power levels, the channel temperature in GFETs on Si/SiO_2 substrates can be up to several hundreds of Kelvin, due to intensive Joule heating, i.e., self-heating effect. This results in degradation of the f_T and f_{max} due to a decrease in the saturation velocity caused by both an increase in the temperature and increase in the thermally generated carrier concentration, see eq. 2.9. A considerable temperature increase in the graphene on SiO_2/Si substrates caused by the self-heating was observed also by other groups of researchers, using infrared microscopy and Raman spectroscopy, even at power densities above 0.1 mW/μm^2 [102, 104], see Fig. 3.12. (from [102]). This indicates the importance of taking into account the effects of self-heating on high-frequency performance, including the gain and noise, in practical circuit applications such as GFET mixers and amplifiers [42,105–107]. Generally, the rise of the transistor channel temperature is directly proportional to the power dissipated (P_{dis}) in the channel as $\Delta T = R_{th} P_{dis}$, where R_{th} is thermal resistance, a parameter defined by both the type and geometry of the materials that compose the structure below the channel. There are several models developed for evaluation of the thermal resistance of the multilayer transistor structures. Dorgan et al.

developed the model using a simple thermal resistance expression, following from the Fourier law of heat conduction [56]. In works by Darwish et al. the maximum channel temperature is calculated based on the solution to the spacial Laplace temperature equation [108]. Bonmann et al. [103] presents theoretical and experimental study of the effects of self-heating and external heating on dc and high-frequency performance of GFETs. In contrast to the studies by other groups, the GFETs considered in this article have the design and layout that are practical for advanced high-frequency applications. Additionally, it is shown that previously developed theoretical models are not readily applicable because they either require the knowledge of the thermal conductivities of the rather complex graphene-substrate layered structures, and/or technology specific temperature-dependent I–V dependencies [109,110]. In Paper Bonmann et al., a novel method was developed for the evaluation of the effective GFET channel temperature, using the measured dependencies of f_{T} and f_{max} on the drain voltage, i.e., dissipated power densities, and at different external temperatures. For this purpose, theoretical expressions for f_{T} and f_{max}, based on small-signal equivalent circuit parameters, are used in combination with the models of the field-dependent carrier velocity and the temperature-dependent and charge carrier concentration-dependent mobility and saturation velocity of GFETs. In contrast to pulsed I–V studies, which are usually employed to investigate thermal effects, all velocity saturation effects, such as optical phonon and remote optical phonon scattering, are included and can be studied under the real application conditions. The method is verified by comparing the values of the thermal resistance found by our method, by employing a thermal-resistance model based on the solution of the Laplace equation [108], and by the method of thermo-sensitive electrical parameters; in particular, the gate leakage current [111]. The self-heating effect can be controlled and minimised, e.g. by optimising the GFETs layouts and/or selecting substrate materials with higher thermal conductivity. Calculations indicate that, because of relatively low thermal conductivity of 1.3 $\mathrm{Wm^{-1}K^{-1}}$, the thermal resistance associated with the SiO_2 layer is up to 80% of that of the total SiO_2/Si substrate. Using the diamond-like carbon (DLC), as a substrate material, even with moderate thermal conductivity of 7 $\mathrm{Wm^{-1}K^{-1}}$, the self-heating temperature rise will be less than 50 K, which will have a negligible effect on the GFET high-frequency performance. For comparison, the thermal conductivity of diamond, which is used as a GFET substrate material in Paper [D], is 1000 $\mathrm{Wm^{-1}K^{-1}}$. As a result, no degradation of the f_{T} and f_{max} were observed at high drain fields.

Chapter 4

Effects of material imperfections on the high-frequency performance of GFETs

This chapter considers intrinsic and extrinsic factors limiting the high-frequency performance of GFETs including zero-bandgap in the electronic band structure of monolayer graphene, graphene/dielectric material imperfections responsible for the low-field elastic charge carrier scattering and inelastic scattering by remote optical phonons of adjacent dielectrics. More detailed analysis of the dependence of high-frequency performance of GFETs on channel transport properties is provided in Paper [A].

4.1 Factors limiting the high-frequency performance of GFETs

Owing to a very high carrier velocity, graphene possesses great potential for high-frequency applications [15, 112]. However, the high-frequency performance of the state-of-the-art GFETs is currently limited by a number of intrinsic and extrinsic factors..

4.1.1 Intrinsic limitations

The main intrinsic limitation of high-frequency performance of GFETs is associated with zero-bandgap in the electronic band structure of monolayer graphene. The zero-bandgap results in ambipolar behaviour of the GFETs without full depletion at the drain side at high drain fields, in contrast to the semiconductor field-effect transistors. In GFETs, instead of full depletion, the region with residual carrier concentration is formed and moves from drain to source with increasing the drain voltage. This region separates parts of the channel with different types of conductivity and results in just rather

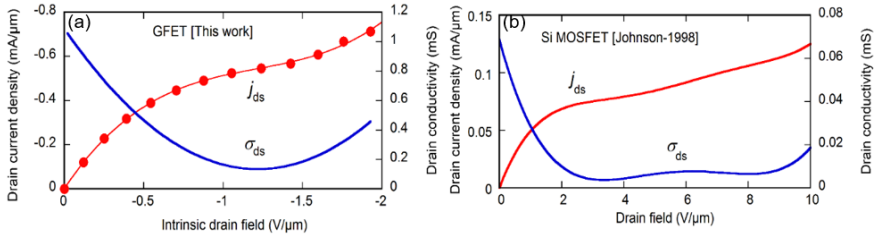


Figure 4.1: (a) Drain current density and differential drain conductivity versus intrinsic drain field of a GFET reported in Paper [A] (b) and a Si MOSFET [99].

short plateau, i.e. kink, in the output characteristics [40]. Subsequently, the drain conductance, which is derivative of the drain current, in GFETs is relatively high. Fig. 4.1 shows the drain current density and drain conductivity, defined as $\sigma_{\rm d}$=$g_{\rm d}/W$, in a GFET presented in Paper [B] in comparison with those of the Si MOSFET counterpart [99]. It can be seen, that the drain conductivity in GFET in the high-field region is more than ten times larger. Analysis of eqs. (3.11)-(3.14) indicates that the high drain conductance limits significantly $f_{\rm max-int}$ and both extrinsic $f_{\rm T}$ and $f_{\rm max}$. Fig. 4.2(a), shows $f_{\rm max}$ experimental and simulated using eq. (3.14). For illustration of the degrading effect of the high $g_{\rm ds}$, the solid line shows the $f_{\rm max}$ simulated using the GFET parameters, the same as those used for fitting the experimental data (upper dotted line), but assuming $g_{\rm ds}$=0.01 mS, which is typical for the Si MOSFETs [99]. It can be seen, that in this case, $f_{\rm max}$ can be as high as 300 GHz at L=200 nm. It was shown, that the bandgap in graphene can be engineered, for example, in graphene nanoribbons or in bilayer graphene applying an out-of-plane electric field. However, as it can be seen from Fig. 4.2(b), it turned out that mobility in graphene decreases with the bandgap even faster than that in the semiconductors. It was concluded, that in terms of mobility and for a given bandgap, graphene does not offer a distinct advantage over conventional semiconductors [29]. Our analysis indicates that a more favourable way to overcome the zero-bandgap issue is a selection of the adjacent dielectric materials with optical phonon energy higher than that of the SiO_2 Paper [A] [37,38,40]. This will increase the saturation velocity limited by the remote phonon scattering, see eq. (2.9) [40,113]. The dashed and dash-dotted lines in Fig. 4.2(a) represent $f_{\rm max}$, simulated using $g_{\rm ds}$=0.3 mS, typical for GFETs, see Fig. 4.1(a), but with graphene encapsulated by Al_2O_3 and hBN layers, respectively. The Al_2O_3 and hBN optical phonon energy are 87 and 100 meV, respectively, resulting in corresponding saturation velocity of approx. $3 \cdot 10^7$ and $5 \cdot 10^7$ cm/s [113]. It can be seen, that the $f_{\rm max}$ of the Al_2O_3 and hNB encapsulated GFETs can be approx. 120 GHz and 180 GHz, respectively, at L=200 nm.

4.1.2 Extrinsic limitations

Extrinsic limitations of the charge carrier transport in GFETs are associated, mainly, with effects of imperfections in graphene, adjacent dielectrics and interfaces. A typical example of imperfection is the polymer residues remaining after the graphene transfer [72] and during the fabrication process, usually

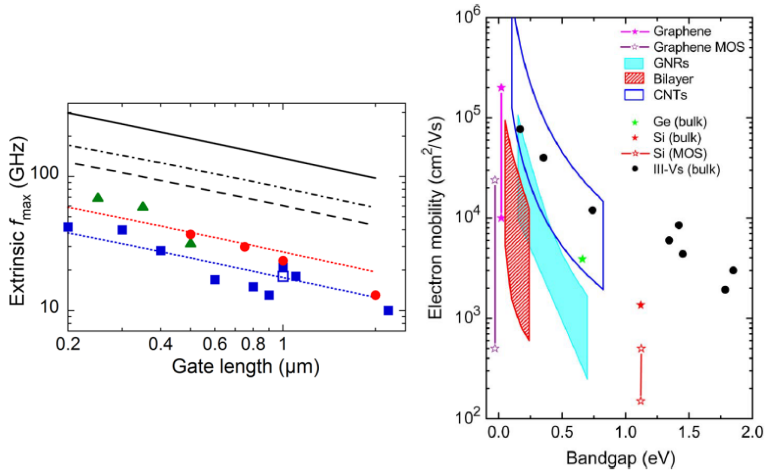


Figure 4.2: (a) Extrinsic maximum frequency of oscillation ($f_{\max}$) versus gate length of GFETs analysed in Paper [B] (circles) shown together with the highest previously published extrinsic $f_{\max}$ of GFETs (squares) and Si MOSFETs (triangles) [41]. The lines are simulations using eq.(3.14). The upper and lower dotted lines correspond to parameters of the GFETs with the highest measured $f_{\max}$ (circle) and our previously published GFET (open square), respectively [37]. The solid line represents $f_{\max}$ of the GFETs assuming $g_{\rm ds}$=0.01 mS, typical for the Si MOSFETs [99]. The dashed and dash-dotted lines represent $f_{\max}$ of the GFETs assuming $g_{\rm ds}$=0.3 mS, but graphene encapsulated by Al_2O_3 and hBN layers, respectively. (b) Mobility versus bandgap of Si, Ge, III-V compounds, carbon nanotubes, mono- and bi-layer graphene and graphene nanoribbons [29].

reduce the carrier mobility below 10,000 cm^2/Vs and also modify the graphene-metal interface in the contact area, which increases the source-drain contact resistances [114, 115]. The effects of the imperfections on the low-field dc graphene properties have been extensively studied theoretically and experimentally. The commonly observed experimental low-field dc characteristics of the graphene devices can be fully described by one or combination of a few mechanisms of the charge carrier scattering including scattering by the charged impurities (also termed as Coulomb or long-range scattering [116]), and the resonant scattering and scattering by the substrate surface polar phonons [66, 117, 118]. The charged impurities are typically associated with oxygen vacancies in the adjacent dielectrics and/or water molecules trapped at the graphene-dielectric interfaces [71, 72]. The resonant scattering in graphene is usually associated with vacancies and adsorbates like H, OH, and CH_3, C_2H_5, CH_2OH [66, 119]. The scattering by the substrate surface polar phonons is associated with the electrostatic coupling of the carriers in graphene to the long-range polarisation field created at the graphene-substrate interface by the substrate phonons [66, 118]. The short-range scattering is caused by defects or dislocations in the graphene lattice and also from the graphene ripples [116]. Apparently, at the current level of graphene-substrate material quality, i.e. concentration of impurities, the scattering by the charged impurities is, usually, the dominating mechanism [66, 120].

According to the self-consistent theory of the charge carrier transport in the graphene, the charged impurities in the substrate and/or graphene-substrate interface create a spatially inhomogeneous screened Coulomb potential [73]. The

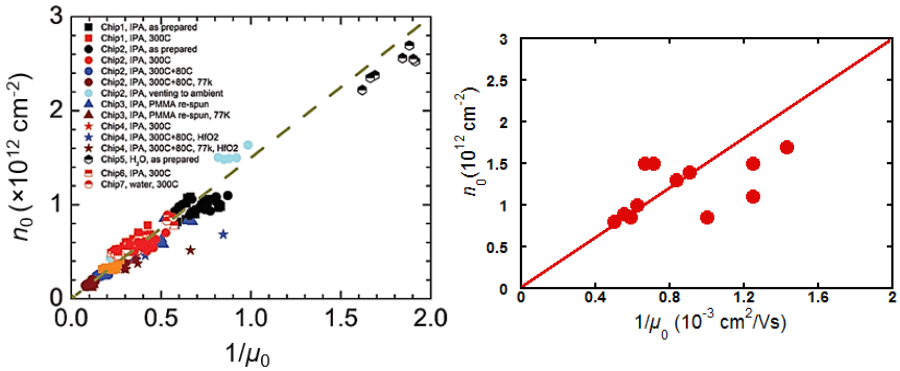


Figure 4.3: (a) Residual charge carrier concentration versus reciprocal of low-field mobility plotted using a large number of characterised devices [121]. (b) Residual charge carrier concentration versus reciprocal of low-field mobility measured on GFETs located at different positions on the Si chip. The line corresponds to the product $\mu_0 \cdot n_0 = 1.5 \times 10^{15}$ 1/Vs Paper [A].

existence of the lateral inhomogeneities in the graphene dc low-field electronic properties associated with the charged impurities is confirmed experimentally by means of the high-resolution, two-dimensional mapping using THz and near-field spectroscopy [66, 122]. A distinguishable feature of the scattering by the charged impurities is that the low-field mobility is defined only by the concentration of impurities and the dielectric constants of the adjacent dielectrics, but does not depend on the carrier concentration [73]. The latter allows for applying the semi-empirical drain resistance model of the GFET and evaluation of the series resistance R_C, low-field mobility μ_0 and residual carrier concentration n_0 as fitting parameters [93].

Low-field mobility and material imperfections

The concentration of impurities plainly defines the residual concentration of the charge carriers, i.e. the concentration at the Dirac point [73]. Therefore, the n_0 found via the drain resistance model can be used as a material quality parameter. The product of the low-field mobility and the residual carrier concentration is constant and, for graphene on the SiO_2 substrate, for example, is $\mu_0 \cdot n_0 = 1.5 \times 10^{15} 1/Vs$ [73]. This relationship is confirmed experimentally for mobilities in the wide range of approx. $10^2 - 10^4 \mathrm{cm}^2/Vs$, see Fig.4.3 (a). Fig. 4.3(b) shows the relationship between the residual charge carrier concentration versus reciprocal of low-field mobility for the GFETs fabricated and studied in paper [A]. The line corresponds to the product of $\mu_0 \cdot n_0 = 1.5 \times 10^{15} 1/Vs$. The general agreement between the experimental dependence and the line confirms that the μ_0 and n_0 distributions are associated mainly with spatially inhomogeneous screened Coulomb potential [116]. However, some mobilities are deviated by the product of $\mu_0 \cdot n_0 = 1.5 \times 10^{15}$ 1/Vs. This indicates additional contributions of the other charge carrier scattering mechanisms, such as 'short-range' or 'resonant' scattering, associated with different scattering mechanisms as discussed above. In this case, the low-field mobility should be used as a more appropriate material quality parameter Paper [A].

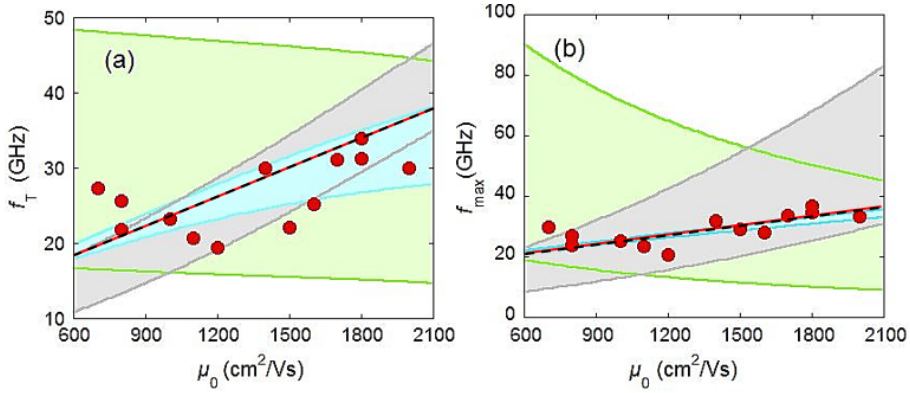


Figure 4.4: Extrinsic transit frequency (a) and maximum frequency of oscillation (b) of the GFETs, located at different positions on the Si chip, versus corresponding values of the low filed mobility. The solid lines are simulations using (3.13)-(3.14), corresponding polynomial dependences of the g_m, g_{ds} and R_c on μ_0 and keeping one of the parameters constant at its highest and lowest values in the studied ranges. The coloured areas between the upper and lower curves correspond to the areas of hypothetical variations of the g_m (grey), g_{ds} (green) and R_C (blue).

4.2 Dependence of high-frequency performance of GFETs on channel transport properties

4.2.1 Relationships between material quality, low-field mobility, equivalent circuit parameters and high-frequency performance

Fig. 4.4 shows the experimentally measured extrinsic f_T and f_{max} of GFETs located at different positions on the Si chip versus corresponding values of μ_0. As can be seen, there are dependencies between the graphene quality and the high-frequency performance of the GFETs. In general, f_T and f_{max} increase in the range of approx. 20-40 GHz with μ_0 varying in the range of approx. 600-2000 cm^2/Vs, which is larger than the deviations from the corresponding simulated dependencies. The solid lines in Fig. 4.4 represent the f_T and f_{max} versus μ_0 simulated using (3.13)-(3.14) and corresponding polynomial dependencies of g_m, g_{ds} and R_C on μ_0 found as fits to experimental data and shown in Paper [A]. Good agreement between the experimental trends and simulated dependencies of the f_T and f_{max} verify the analytical expressions of f_T and f_{max}, as well as the models used for calculations of the g_m, g_{ds} and R_C. The dotted lines in Fig. 4.4 are linear fits to the simulations. The simulated f_T and f_{max} dependencies on μ_0, in the studied mobility range, can be well approximated by linear functions of $f_T(\mu_0) = A_1 + B_1\mu_0$ and $f_{max}(\mu_0) = A_2 + B_2\mu_0$ with coefficients A_1=10 GHz, A_2=16 GHz, $B_1 = 1.3 \cdot 10^{-11} V/cm^2$ and $B_2 = 9.5 \cdot 10^{-12} V/cm^2$. The approximations can be used for the evaluations and predictions of the f_T and f_{max}, in the studied mobility range and in the vicinity, using the low-field mobility only found from the GFET DC transfer characteristics, i.e. without measuring the S-parameters. For instance, extrapolations to μ_0=5000 V/cm^2 give f_T=75 GHz and f_{max}=64 GHz for the GFETs of similar design.

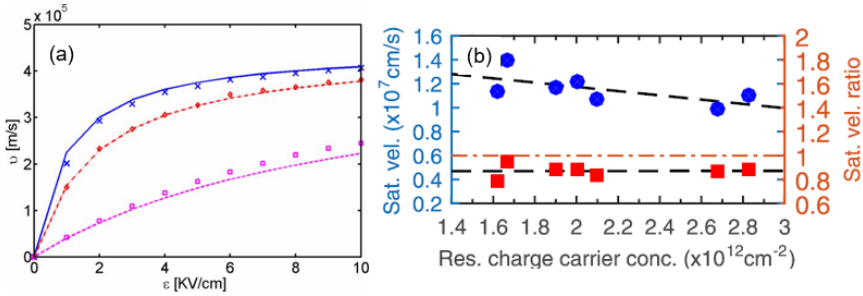


Figure 4.5: (a) The average carrier velocity vs. the electric field at different impurity concentrations, n_{imp}=0 (crosses), $10^{11}\mathrm{cm}^2$ (diamonds), and $10^{12}\mathrm{cm}^2$ (squares), found by the Monte Carlo simulations and fitted by the Canali model The carrier concentration was fixed at n=$5.29{\cdot}10^{12}\mathrm{cm}^2$ and the energy of the OP was $\hbar w_{\mathrm{OP}}$=200 meV [113]. (b) Saturation velocity, calculated using Canali model (circles), and its ratio to effective saturation velocity is calculated using eq. (2.9) considering graphene with SiO_2 OPs (squares) vs. the residual charge carrier concentration (n_0) [37].

Thus, the established correlations clarify the ways of further development and improvement of GFET high-frequency performance.

The established correlations between the f_{T}, $f_{\max}$, g_{m}, g_{ds}, R_{C} and the low-field mobility allow for analysis of the relative effects of the equivalent circuit parameters on the high-frequency performance of the GFETs. For demonstration, Fig. 4.4 shows the experimentally measured f_{T} and $f_{\max}$ versus μ_0 together with the simulation curves calculated using (3.13)-(3.14) and corresponding polynomial functions of the g_{m}, g_{ds} and R_{C}, while keeping one of the parameters constant at its highest and lowest values in the studied ranges. The g_{m}, g_{ds} and R_{C} varies between the hypothetical values of 5 mS to 13.5 mS, 7.5 mS to 33 mS and 11 Ω - 22.5 Ω, respectively. The coloured areas between the upper and lower curves correspond to the areas of hypothetical variations of specific parameters. In particular, the upper and lower curves of the g_{ds} and R_{C} variation areas correspond to their lowest and highest values, while the upper and lower curves of the g_{m} variation area correspond to its highest and lowest values, respectively. As can be seen, the variations of the R_{C} in the studied range have relatively weak effects on the f_{T} and, especially, $f_{\max}$. This can be explained by the extremely low contact resistance in our GFETs. One can see from Fig. 4.4 that variations in the f_{T} and $f_{\max}$ are mainly governed by corresponding variations in the g_{ds} and g_{m}. Apparently, for the higher f_{T} and $f_{\max}$ the lower g_{ds} and higher g_{m} are required. Our analysis indicates that a more favourable way is increasing the g_{m} via selection of the adjacent dielectric materials with optical phonon energy higher than that of the SiO_2. This will increase the saturation velocity limited by the remote phonon scattering [57]. For example, the Al_2O_3 and hBN optical phonon energies are 87 and 100 meV, respectively, resulting in corresponding saturation velocity of approx. $3 \cdot 10^7$ cm/s and $5 \cdot 10^7$ cm/s [57]. It can be shown that the $f_{\max}$ of the Al_2O_3 and hBN encapsulated GFETs can be approx. 120 and 180 GHz, respectively, at L_{g}=200 nm.

4.2.2 Effects of material imperfections on the high-field drift velocity

In contrast to the rather extensive studies on the charge carrier scattering in graphene at low fields, considered in above sections, the previous research on correlations between material imperfections and high-field drift velocity are very limited. It is assumed, that at high fields the charge carrier transport is governed by the inelastic soft optical phonon (OP) scattering induced by the graphene and/or adjacent dielectrics [40, 113]. The effect of impurities is considered only via variations in the low-field mobility. In particular, Fig. 4.5(a) shows the average carrier velocity versus the electric field found by the Monte Carlo simulations and fitted by the Canali model, see eq. (2.8), at different impurity densities [113]. The low-field mobility μ_0, which is assumed to be limited by the elastic acoustic phonon (AP) scattering and charge impurity scattering, was obtained from the slope of the velocity versus field curve at a low field. The saturation velocity was obtained using a linearisation approximation:

$$v_{sat} = v_F \frac{\hbar w_{OP}}{E_F} = \frac{2}{\pi} \frac{w_{OP}}{\sqrt{\pi n}}, \tag{4.1}$$

where E_F is the equilibrium Fermi level, $\hbar w_\mathrm{OP}$ is the OP energy and n is the carrier concentration. The carrier concentration was fixed at n=$5.29\times10^{12}\mathrm{cm}^{-2}$ and the energy of the OP was $\hbar w_\mathrm{OP}$=200 meV, corresponding to that of graphene. It was concluded, that the transport property is insensitive to the inelastic scattering rate, but it is sensitive to the energy of the inelastic phonons and the elastic scattering rate. In Ref. [37] an attempt was made to take into account also the OP scattering associated with the phonons induced by the charged impurities. The effective saturation velocity ($v_{\mathrm{sat-eff}}$) defined by several different OP mechanisms was introduced and Matthiessen's rule [65] applied as:

$$v_{\mathrm{sat-eff}}^{-1} = v_{\mathrm{sat-G}}^{-1} + v_{\mathrm{sat-SiO_2}}^{-1} + v_{\mathrm{sat-Al_2O_3}}^{-1} + v_{\mathrm{sat-n_0}}^{-1}. \tag{4.2}$$

where $v_{\mathrm{sat-G}}$ is the saturation velocity limited by the graphene zone-edge OPs, $v_{\mathrm{sat-SiO_2}}$ and $v_{\mathrm{sat-Al_2O_3}}$ are the saturation velocities limited by the surface OPs of the SiO_2 substrate and the Al_2O_3 gate dielectric, and $v_{\mathrm{sat-n_0}}$ is the saturation velocity associated with OPs of the impurities. Fig. 4.5(b) shows the saturation velocities, calculated from the transit delay (circles) using Canali model, of GFETs versus residual carrier concentration. It can be seen that there is a clear correlation, i.e., v_sat decreases with n_0. However, the normalised saturation velocity does not show apparent dependence on n_0, see Fig. 4.5(b). This indicates that, within the range of residual charge carrier concentrations considered in this work, most likely the OPs of impurities do not contribute to the inelastic scattering of the charge carriers at high fields.

Chapter 5

Impact of adjacent dielectrics on the high-frequency performance of GFETs

In this chapter, the GFETs with enhanced high-frequency performance utilising dielectric materials with high optical phonon energy are considered. The model of inelastic remote phonon scattering is introduced and its effects on f_{T} and f_{max} are analysed. It is shown, that adjacent dielectric materials with relatively high OP energies are favourable for RF GFETs. The diamond is selected as most promising gate dielectric and substrate material and performance of state-of-the-art diamond GFETs is analysed.

5.1 Effects of adjacent dielectrics on f_{T} and f_{max}

Owing to extremely high intrinsic velocity of charge carriers, graphene is being considered as a channel material for a novel type of transistor with scaling limits and operating speeds higher than those of conventional semiconductors. However, it turned out that the carrier velocity in graphene field-effect transistors is limited significantly by the inelastic scattering of the relatively low-energy surface optical phonons (OPs) of the adjacent dielectrics [44, 56, 113, 123]. For instance, the OPs energy of SiO_2, commonly used on top of the Si substrates, is in the range of 50–60 meV, which is much less than the 160-200 meV of graphene zone-edge OPs and, therefore, limits the charge carrier velocity in graphene [113, 124]. As a result, the two main high-frequency FOMs, i.e. the f_{T} and f_{max}, characterising, respectively, the transistor current and power gain, are significantly reduced. It was clearly understood, that the low-field mobility in GFETs is strongly reduced, in comparison with the intrinsic value, by a number of extrinsic scattering mechanism [66]. In contrast to the low-field mobility, the high-field velocity of the charge carriers in graphene did not attract much attention and was the least investigated. However, the analysis indicates that

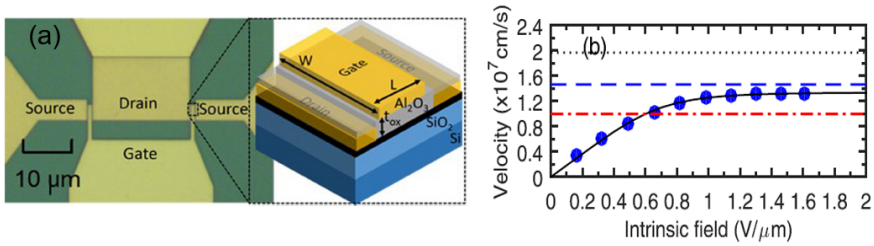


Figure 5.1: (a) Optical micro-photo and schematic view of a GFET gate region. (b) Carrier velocity found via delay time analysis (circles) and fitted by the drift velocity model (solid line). The other lines represent saturation velocities simulated for combinations of optical phonons of graphene with Al2O3 (dotted), SiO2 (dashed), and both Al2O3 and SiO2 (dashed-dotted) [37].

it is the high-field velocity, and, in particular, the saturation velocity v_{sat}, that defines the high-frequency performance of GFETs. As defined previously, the high-frequency FOMs of any FETs can be expressed via carrier drift velocity v_{d} as eqs. (3.3) and (3.4): It follows from (3.3), (3.4) and (2.8) that the higher f_{T} and f_{max} can be achieved with higher v_{sat}. Appreciation of these relationships allowed researchers, including the author of this thesis, to develop GFETs with state-of-the-art extrinsic f_{T} and f_{max}, up to above 50 GHz Paper [C] and [D].

For the first time, it was shown in the work by Meric et al., that at the high-fields the charge carriers in graphene on SiO_2/Si substrates are predominantly scattered by remote SiO_2 OPs [40]. It was suggested that the saturation velocity in future generations of GFETs may be augmented by choosing different substrates with higher OPs energies [40]. The model of v_{sat} limited by inelastic emission of OPs was developed in the work by Dorgan et al. including the roles of carrier concentration and temperature as [56]:

$$v_{sat} = \frac{2}{\pi}\frac{w_{OP}}{\sqrt{\pi n}}\sqrt{1-\frac{w_{OP}^2}{4\pi n {v_f}^2}}\frac{1}{N_{OP}+1}. \tag{5.1}$$

Here, $\hbar w_{\mathrm{OP}}$ is the optical phonon energy, $N_{OP} = 1/[exp(\hbar w_{OP}/kT) + 1]$ is the phonon occupation, k is the Boltzmann constant and n is the charge carrier concentration. The model was verified by characterisation of back-gate graphene Hall-bar test structures on SiO_2/Si substrates. It was found that both the graphene zone-edge and SiO_2 substrate OPs play a role in limiting v_{sat}, but that substrate OPs are dominant. Therefore, the intrinsic graphene saturation velocity could be more than twice that observed [56].

5.2 Dielectric materials with high optical phonon energy for high-frequency GFETs

The model of saturation velocity was applied in previous studies by our lab for the analysis of top-gated GFETs, with Al_2O_3 gate dielectric, on SiO_2/Si substrates (see Fig. 5.1) [37]. It was assumed that the effective saturation velocity is defined by combined inelastic emission of OPs of the graphene and both adjacent dielectrics, and applied Matthiessen's rule for the velocity

analysis. It was concluded that only the combination of the graphene and SiO_2 OPs gives a good agreement with the velocity experimentally found using the delay time analysis [37].

Replacing both the SiO_2 substrate and Al_2O_3 top-gate dielectric with materials with higher OP energies was suggested. For instance, according to the calculations, sandwiching graphene between hBN, material with OPs energy of 101 meV, i.e. almost two times higher than that of the SiO_2, allows for increasing the saturation velocity up to $3{\cdot}10^7$ cm/s [41, 42]. In Paper [B], the GFETs demonstrated, still fabricated on SiO_2 substrate and with the Al_2O_3 gate dielectric, but with improved quality of the graphene and adjacent dielectrics, which allowed us to minimise emission of carriers from traps and, hence, achieve the drain current saturation trend following that of the velocity [42]. This resulted in the state-of-the-art extrinsic f_T and f_{max} up to 40 GHz at the 0.5 μm gate length. In this work, it was proposed replacing the SiO_2 by Al_2O_3 with higher OPs energy of 87 meV, since it can be readily realised with the developed technology. This idea was validated experimentally in Paper [C], where GFETs were fabricated and characterised with Al_2O_3 gate dielectric and Al_2O_3 buffer layer between the graphene channel and SiO_2/Si substrate. The work by Oh et al. reported GFETs with Al_2O_3 top-gate dielectric and AlN bottom buffer layer, which is material with OPs energy of 84 meV, i.e. also higher than that of SiO_2/Si substrate [125]. The intrinsic f_T was reported to be 115 GHz at 50 nm gate length, significantly higher than that of 55 GHz of the control GFET without AlN buffer layer. The SiC, which is typically used as a substrate for epitaxial growth of graphene, is a material with relatively high OP energy of 116 meV [34, 125]. This partly explains enhanced high-frequency performance usually observed in the GFETs using epitaxial graphene. In particular, Yu et al. reported GFET fabricated on quasi-freestanding bilayer epitaxial graphene grown on SiC (0001) substrate and with Al_2O_3 top-gate dielectric, which exhibited extrinsic f_T of 50 GHz and f_{max} of 40 GHz at gate length of 200 nm [35]. In the two latter works, the authors did not associate directly the enhanced high-frequency performance with the higher OP energy of the used substrates. However, the results confirm the limiting effect of the inelastic remote phonon scattering on the carrier velocity in the graphene channel. Further analysis indicates that the material of choice for dielectrics adjacent to the graphene channel is diamond, of which OP energy is comparable or even slightly higher than that of the graphene zone-edge OPs [32, 33].

5.3 GFETs with graphene channel encapsulated by Al_2O_3 layers

The approach of encapsulating the graphene channel by Al_2O_3 layers, proposed in Paper [B] was validated experimentally, for the first time, in our recent work presented in Paper [C]. The work was motivated by the reported OP energy of Al_2O_3 of 87 meV, which is up to 40% higher than that of 50-60 meV of the SiO_2 [123, 124]. In Paper [C], GFETs using Al_2O_3 gate dielectric with and without Al_2O_3 buffer layer between the graphene channel and SiO_2/Si substrate where fabricated and characterised as shown Fig. 5.2. The GFETs with the

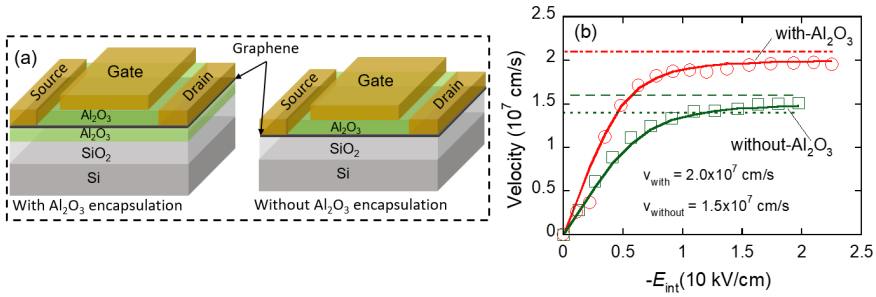


Figure 5.2: (a) Cross-sectional schematic views of gate region and (b) charge carrier velocity versus electric field in GFETs with and without Al_2O_3 buffer layer. Paper [C]

Al_2O_3 buffer layer, measured in Paper [C], revealed extrinsic f_T and f_{max} up to 43 GHz and 46 GHz, respectively, at 0.5 μm gate length, which are approx. 30% higher than those of state-of-the-art GFETs with similar gate length. The improvement found compared with GFETs on SiO_2 is explained mainly by the higher OP energy of the encapsulating material resulting in a higher charge carrier saturation velocity. The delay time analysis showed that the charge carrier saturation velocity increased from $1.5{\cdot}10^7$ cm/s to $2{\cdot}10^7$ cm/s in GFETs without and with Al_2O_3 buffer layers, respectively. It was concluded that in addition to scaling of the gate length, one road ahead for further progress in high-frequency GFET performance might be to use the substrate and gate dielectrics with even higher optical phonon energies. Analysis indicates that the most promising candidate is the diamond or diamond-like layers.

5.4 GFETs on diamond substrates with enhanced high-frequency performance

Further analysis indicates that the material of choice for dielectrics adjacent to the graphene channel is diamond or diamond-like carbon (DLC), materials with OP energies up to 165 meV, which is comparable or even slightly higher than that of the graphene zone-edge OPs [126, 127]. Therefore, the carrier velocity in GFETs with the graphene channel encapsulated by diamond-like layers will be entirely defined by the intrinsic graphene OPs, i.e. not limited by the remote phonons of adjacent dielectrics. Another advantage of using diamond or DLC as a high-frequency GFET substrate material is their high thermal conductivity (k). The k of diamond is approx. 2000 $Wm^{-1}K^{-1}$, which is the highest among all other dielectric materials. The k of DLC can be up to 20 $Wm^{-1}K^{-1}$, depending on density, which is still much higher than 1.3 $Wm^{-1}K^{-1}$ of SiO_2. It was shown in Paper [C] and Paper [E] that the high thermal conductivity of substrate is a crucial property of GFETs for high-frequency applications [42, 128]. At relatively high drain fields, above approx. 1 V/μm, required for the carrier velocity saturation, the channel temperature in GFET on SiO_2/Si substrate can be as high as 600 K, due to intensive Joule heating provoked by the low thermal conductivity of the SiO_2 layer. According to eq. (5.1), both the increase in temperature and the following increase in the carrier concentration caused by thermal generation,

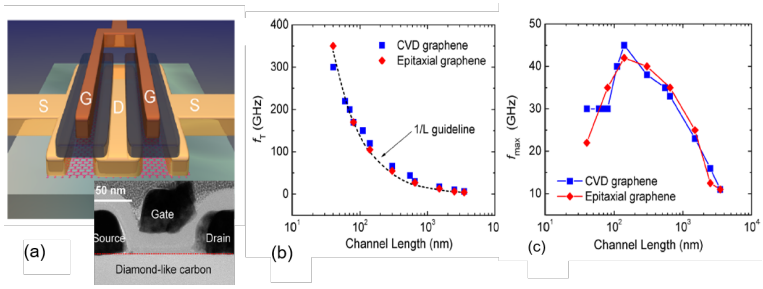


Figure 5.3: High-frequency GFETs on DLC/Si substrates. a) Schematic view with inset showing a cross-section TEM image of a gate region. (b) Intrinsic $f_{\mathrm{T-int}}$ and (c) intrinsic $f_{\mathrm{max-int}}$ versus channel length [33].

result in the reduction of the saturation velocity and, hence, degradation of the high-frequency performance of the GFETs [103]. Preliminary calculations show that with using the DLC even with moderate k of 7 $\mathrm{Wm^{-1}K^{-1}}$, the self-heating temperature rise will be less than 50 K, which has a negligible effect on the GFET high-frequency performance. Yu et al. demonstrated dc performance of GFETs and graphene test structures on single-crystal diamond and ultrananocrystalline diamond substrates [129]. It was shown, that, due to higher thermal conductivity of the substrates, the current-carrying capacity of graphene can be substantially increased up to as high as 18 $\mu\mathrm{A/nm^2}$ achieving the graphene intrinsic current-carrying capacitance limit. This work is the only publication to date on the GFETs on single-crystal diamond substrates.

5.4.1 GFETs on diamond-like carbon

Wu et al. demonstrated, for the first time, high-frequency performance of GFETs on the DLC/Si substrates, see Fig. 5.3, clearly motivating the work by the advantage of the high phonon energy in sp3-hybridized carbon [32, 33]. As a result of this advantage, the GFETs revealed excellent state-of-the-art intrinsic $f_{\mathrm{T-int}}$ up to 300 GHz at 40 nm gate length, Fig. 5.3(b), surpassing previous records of any GFETs [32]. The intrinsic $f_{\mathrm{max-int}}$ was found to be up to 45 GHz at the gate length of 140 nm, Fig. 5.3(c), which is also record high in spite of being limited by the relatively high gate resistance. To the best of the author's knowledge, the papers by Wu et al. are the only publications, so far, on high-frequency performance of GFETs on diamond or DLC substrates.

5.4.2 GFETs on single crystal diamond

State-of-the-art GFETs on single-crystal diamond substrate with extrinsic f_{T} and f_{max} up to 55 GHz are reported in Paper [D]. To the best of the author's knowledge these are the highest values reported so far for the GFETs. Fig. 5.4 shows extrinsic f_{T} and f_{max} versus gate length. The effective drift velocity of the charge carriers versus intrinsic drain field, found from the drain current versus intrinsic drain field dependence, and the saturation velocity versus the carrier concentration are shown in Fig. 3.8. Comparison with the GFETs on the $\mathrm{Si/SiO_2}$ substrates indicates that the saturation velocity, extracted from

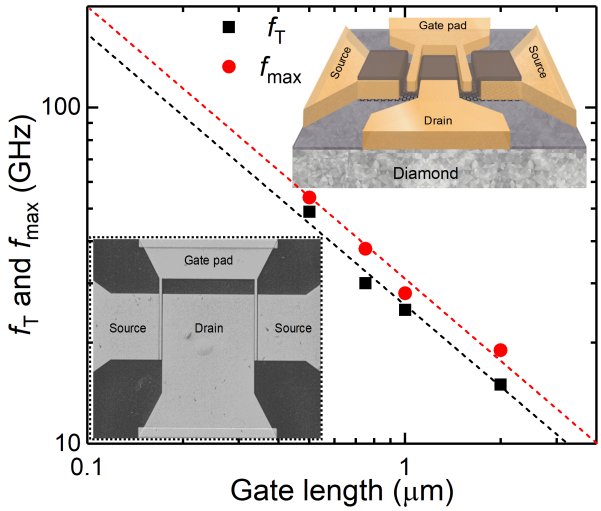


Figure 5.4: Extrinsic transit frequency (f_T) and maximum frequency of oscillation (f_{max}) versus gate length of GFETs on diamond substrate reported in Paper [D]. Inset shows the 3D schematic views GFET and the SEM image of a top-gated dual-channel GFET.

the drain current density versus field dependence, increased from $2.2 \cdot 10^7$ cm/s up to $3.7 \cdot 10^7$ cm/s, which is the highest reported for top-gated GFETs.

5.4.3 State-of-the-art GFETs

In recent years, remarkable efforts have been made to develop GFETs with competitive high-frequency performance, including the attempts of scaling down of the gate length and addressing both intrinsic and extrinsic limitations. Fig. 5.5 shows the extrinsic f_{max} versus gate length of GFETs on diamond substrates presented in Paper [D] in comparison with the best reported f_{max} of the CVD, exfoliated and epitaxial GFETs on Si, SiC and DLC substrates [33–36, 42, 130] and the FETs based on other classes of 2D materials including black phosphorus [46, 59, 131], MoS2 [58, 132, 133] as well as carbon nanotubes [48, 131, 134] and MOSFETs [99–101]. It can be seen, that the extrinsic f_{max} of the GFETs on diamond substrates developed in Paper [D] exceeds that of the best published GFETs. It can be seen also that, in contrast to the most of the other GFET and 2D technologies, the GFETs on diamond substrates reveal a persistent scaling down behaviour similar to that of MOSFET and well-described by the $1/L$ dependence. The scaling down extrapolation indicates that the f_{max} as high as 200 GHz at 100 nm gate length can be expected.

For analysis of dependences of the gate capacitance (C_G) and transconductance (g_m) on the high-frequency performance of state-of-the-art transistors fabricated by different technologies, Fig. 5.6(a) shows reciprocal of the net gate capacitance versus the transconductance normalised by the channel width. The dashed lines represent different f_{T-int} given by the relationship of f_{T-int}=$g_m/2C_G$. The circles represent performance of different state-of-the-art technologies including the GFETs, CNT FETs, CMOS and HEMTs with different gate lengths, which has been reported over the past few years. For correct

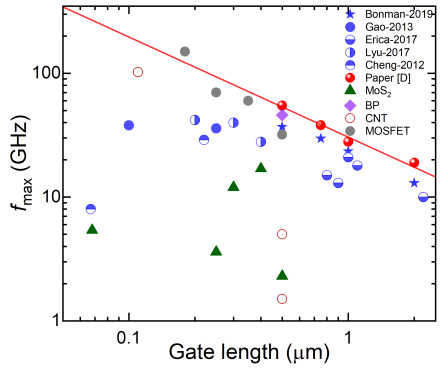


Figure 5.5: Maximum frequency of oscillation ($f_{\max}$) vs. gate length (L). Extrinsic $f_{\max}$ versus gate length shown by solid red circles is this work. The solid line showing $1/L$ dependence demonstrates the scaling behaviour of these GFET devices. For comparison, also shown are the $f_{\max}$ performance of CVD, exfoliated and epitaxial graphene FETs on Si, SiC and carbon-like-diamond substrates [34–36, 42, 130] and the FETs of other similar class of 2D materials such as black phosphorus [46, 59, 131], MoS_2 [58, 132, 133] as well as carbon nanotubes [48, 131, 134]. Also shown are $f_{\max}$ of MOSFET in the similar gate length range [99–101].

comparison of the FETs having different geometries and layouts, both the gate capacitance and transconductance are normalised by the gate width. The $f_{\mathrm{T-int}}$ shown in Paper [D] is up to 100 GHz for 0.5 μm gate length. Analysis of the plot indicates that the $f_{\mathrm{T-int}}$ cannot be increased by varying the oxide capacitances and, therefore, scaling of the gate oxide thickness may not help in improving the RF performance of GFET. Overall, it can be seen that the intrinsic $f_{\mathrm{T-int}}$ of GFETs is comparable with that of the CMOS technology at similar gate length. The $f_{\mathrm{T-int}}$ of HEMTs is significantly higher mainly because of much shorter gate length. Fig. 5.5(b) gives more correct benchmarking of the high-frequency performance of the GFETs on diamond substrates presented in Paper [E] by plotting extrinsic $f_{\max}$ versus f_{T} of different technologies of transistors with the same gate length of a 0.5 μm. It can be seen, that GFETs presented in Paper [D] reveal the highest f_{T} and $f_{\max}$. Fig. 5.5(b) also shows significant improvement in the GFET high-frequency performance achieved for the past years via technological development, and, in particular, selection of the adjacent dielectric materials with higher OP energy. One can expect further significant increase in f_{T} and $f_{\max}$ by scaling the gate length down to deep sub-μm range.

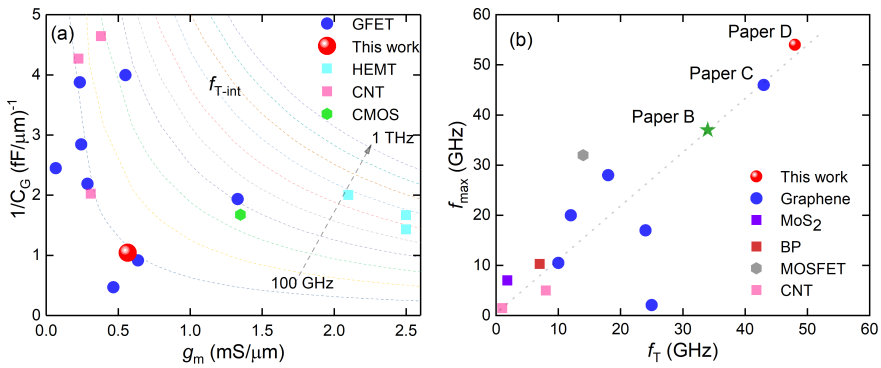


Figure 5.6: (a) The reciprocal of the net gate capacitance C_G versus the transconductance g_m normalised with the channel width. The dashed lines are obtained using the expression of $f_{T-int} = \frac{g_m}{2\pi C_G}$. The intrinsic f_{T-int} performance of GFETs [32, 34, 35, 48, 130, 135] and other established FET technologies like CMOS [50], CNT [136–138] and HEMTs [139–141] of different gate lengths are shown also for comparison. (b) Benchmarking the different RF FET technologies by extrinsic maximum frequency of oscillation (f_{max}) and transit frequency (f_T) of similar gate lengths. Extrinsic f_{max} versus f_T of GFETs presented in Paper [D] for 0.5 μm gate length [42, 43]. It is compared with other GFET fabricated using CVD, epitaxial and exfoliated graphene [30, 32, 35, 44, 45]. It is also compared with the FETs of other 2D materials BP and MoS_2 [46, 47], CNT [48, 49] and MOSFET [50] of similar gate lengths.

Chapter 6

GFET IC amplifiers

In this chapter, status and perspectives of the GFET RF amplifiers are considered and analysed. The motivation of the selected design approach and features of fabrication technology of the X- and Ku-band GFET fully integrated circuit amplifiers presented in Paper [G] are described. The characterisation and performance analysis of the fabricated amplifiers are briefly discussed.

6.1 GFET RF amplifiers: status and perspectives

Fig. 6.1 shows a simplified block diagram of a heterodyne receiver. The ultimate goal is development and fabrication of the integrated receiver entirely based on GFETs, which will allow the exploitation of all of graphene's unique properties. Some parts of the receiver based on GFETs have been already developed and successfully demonstrated, including IF amplifier, sub-harmonic mixers and detectors [16–18, 23, 24, 142, 143]. Development and fabrication of the RF amplifier based on GFETs is a more challenging task, because it requires GFETs with state-of-the-art extrinsic f_{T} and f_{max}. That is why, progress in the development of the GFET RF amplifiers is relatively low. Only a few studies have been published reporting successfully implementing of GFETs as an amplifier [24, 25, 27]. From the RF amplifier design point of view, the values of f_{T} and f_{max} of active circuits should be several times higher than the designed operational frequency of an amplifier in order to achieve a decent gain with practical matching circuitry. This thesis shows important developments in the improvement of f_{max} with promising scaling down behaviour predicting the f_{max} reaching up to 100 GHz and, hence, the possible use of GFET for millimeter wave communication systems [42, 144].

The first matched small-signal amplifier was demonstrated by Andersson et al. from our group in 2012 with a gain up to 10 dB at 1 GHz [24]. A gain of 1.5 dB at 0.2 GHz was presented in 2015 by Ref. [26]. Another serious effort was made by Yu et al. in 2016 using a bilayer graphene FET IC amplifier with integrated micro strip lines design on SiC substrate reported in [27] with a gain of 3.4 dB at 14.3 GHz. Very recently, a C-band graphene low-noise amplifier was demonstrated by the same group showing a maximum gain of 8.34 dB at

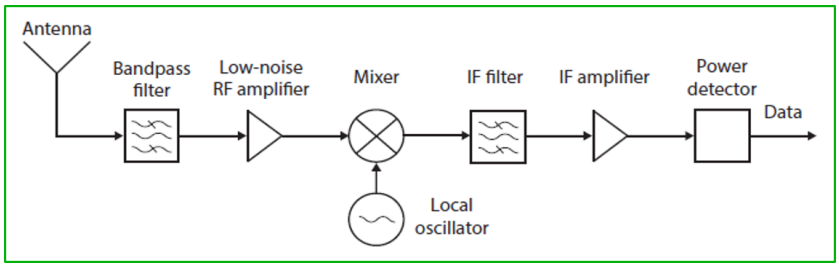


Figure 6.1: Simplified block-diagram of heterodyne receiver.

Table 6.1: Comparison of 2D-material FET amplifiers.

Technology	Gain (dB)	Freq. (GHz)	Ref.
GFET	10	1	[24]
GFET	3.4	14.3	[27]
GFET	6-7	0-3	[145]
GFET	4.8	2.4	[146]
GFET	8.3	5.5	[28]
GFET	4.2	11.4	**This work**
MoS_2 FET	15	1.2	[47]
BP FET	40	1	[147]

5.5 GHz [28]. Omid et al. also showed a wide-band GFET amplifier using epitaxial graphene on a SiC substrate for frequency range 0-3 GHz and the gain reached 6-7 dB [16]. Table 6.1 comprises the established performance of GFET and other 2D-material FET amplifiers. Nevertheless, the further technological developments towards higher frequencies requires GFET with higher f_{max} but also a robust design and matching circuitry that can accommodate emerging 2D material FET devices.

6.2 X- and Ku-band GFET IC amplifiers with state-of-the-art performance

6.2.1 Technology tolerances and matching network design

Challenging but successful development of the GFETs with state-of-the-art extrinsic f_T and f_{max} above 30 GHz enabled realisation of the X and Ku-band IC amplifiers presented in Paper [G]. However, another key challenge for the GFET amplifier was identified at the circuit designing level. Like any other emerging device technologies, graphene transistors are also facing device to device variations in parameters, and performances caused by the uncontrolled extrinsic factors, first of all, spatially distributed imperfections in the graphene, adjacent dielectrics and interfaces [38]. This raised challenges from the circuit design perspective. As an example, Fig. 6.2 shows the maximum available gain (MAG) of 13 GFET devices fabricated in this work, situated at different positions on a Si chip, plotted versus device index. The MAG was calculated

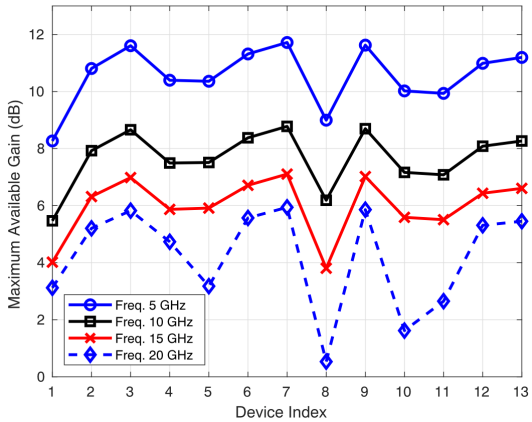


Figure 6.2: Extracted maximum available gain of the GFETs fabricated in this work.

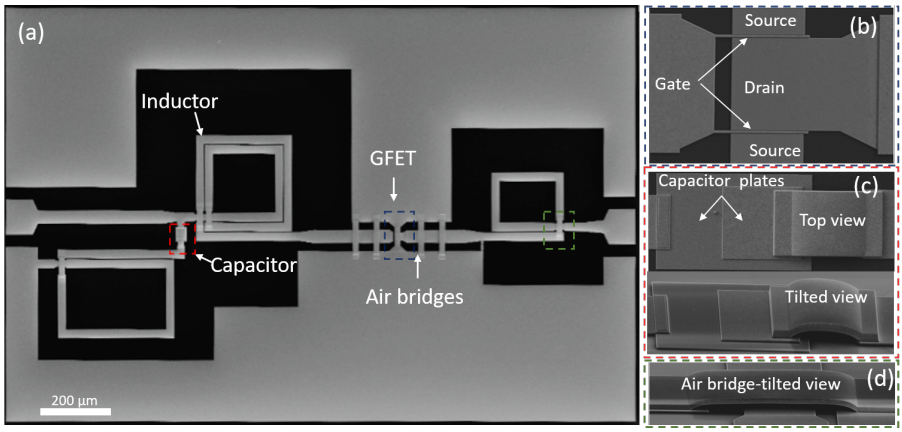


Figure 6.3: (a) SEM image of a 15 GHz GFET amplifier integrated circuit, (b)-(d) magnified SEM images of the GFET, capacitor and air bridges corresponding to the dashed boxes in (a).

from the S-parameters measured at the optimum bias point for each device with the aim of achieving highest f_{T} and f_{max}. The extracted MAG varies across devices and also with frequency as anticipated. However, fully integrated designs, models and methodologies require prior knowledge of active device parameters to obtain predictable and reproducible device performance. To overcome the wide variations of the GFETs, as well as the high isolation (S12), the negative-image equivalent circuit technique was employed during the circuit design [148, 149]. Negative image technique aided designing input output matching network over a wide frequencies range. Moreover, the design methodology allows for optimising the matching network, which can tolerate device S-parameters variations to a certain extent and offer optimal gain and bandwidth.

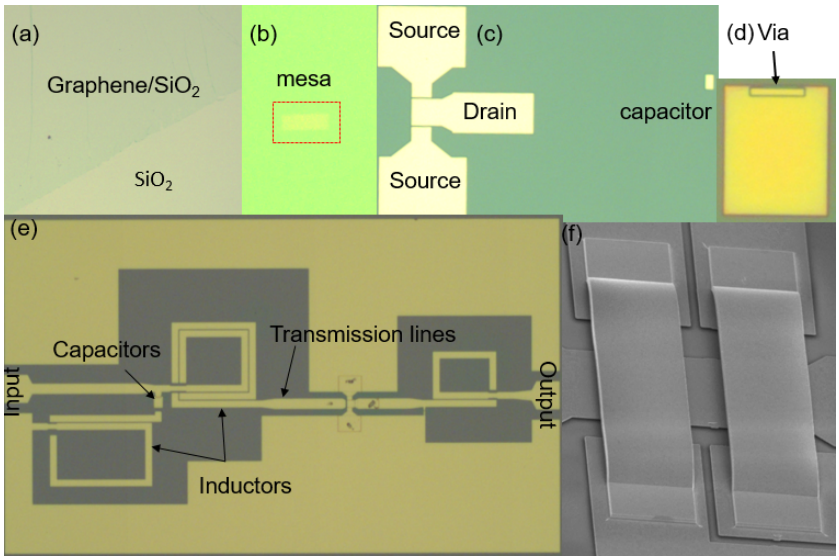


Figure 6.4: Micro-photos of the IC components at certain fabrication steps as follows: (a) graphene transferred on a Si/SiO2 substrate, (b) graphene/dielectric mesa, (c) source/drain contacts and bottom metal plates of capacitors, (d) via holes (e) inductors, transmission lines, top plates of capacitors (f) air bridges.

6.2.2 Technology development

Fig. 6.3 shows SEM image of a fully integrated RF GFET IC amplifier. The IC consists of a GFET and passive components integrated on a Si chip within 1.6 mm^2 area. The passive components include integrated capacitors, inductors, transmission lines, vias and air bridges. Usually, ICs are fabricated using two basic processing approaches: i) back-end of line process and ii) frond-end of line process. Back-end of line process flow starts with formation of the active circuit components and finishes with fabrication of the passive components. In contrast, the front-end of line process starts with passive components and finishes with the active components. Both processes have certain advantages and disadvantages depending on the selected IC design and technology [112]. For fabrication of the GFET IC amplifiers presented in Paper [G], a different approach has been developed and used. This approach allows for fabrication of the IC's active and passive components simultaneously, i.e. during the same lithography steps. This allows for minimising the number of lithographic steps and, hence, increasing the performance of the GFETs and entire ICs. Following are the main steps of fabrication of the GFET IC amplifiers.

• CVD graphene is transferred on to high resistivity silicon substrates covered by 1 μm thick thermally grown SiO_2, as shown in Fig. 6.4 (a).

• A graphene channel is protected by 5 nm thick thermally oxidised Al_2O_3 dielectric, subsequently, used as a gate dielectric. This provides encapsulation of graphene and, hence, minimises the degradation of the performance during the next processing steps.

• Graphene/dielectric mesa is patterned, as shown in Fig. 6.4 (b).

• Source/drain contacts and bottom plate of capacitors are fabricated by depositing Ti/Pd/Au (1 nm/15 nm/285 nm) layer stacks, as shown in Fig.

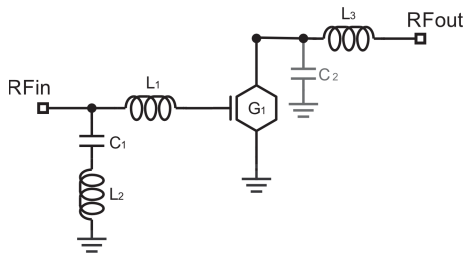


Figure 6.5: Equivalent circuit of the GFET IC amplifiers.

Table 6.2: Values of the passive components of the fabricated GFET amplifier.

Component	Value	Component	Value	Component	Value
C_1 (pF)	2.65	C_2 (pF)	1.30	L_1 (nH)	2
L_2 (nH)	0.7	L_3 (nH)	0.8		

6.4 (c). Detail of high quality metal-graphene contact formation are described earlier and in Ref. [38].
• The gate oxide and capacitor insulator dielectric is deposited in the same step by forming first 5 nm thick thermal oxidised Al_2O_3 seed layers followed by 12 nm thick Al_2O_3 deposited by atomic layer deposition (ALD) technique.
• The via is etched using wet chemical etching process in order to make electric contact with the bottom metal plate which is covered now with oxide layer. One of the via holes is shown in Fig. 6.4 (d).
• The gate fingers, top plates capacitors, inductors, transmission lines and the integrated source, drain pads are realised in the next step by depositing Ti/Au (100nm/300nm) metal layers and can be seen in Fig. 6.4 (e).
• Finally air bridges are constructed using bridges lithography, as shown in Fig. 6.4 (f). Bridge lithography is very crucial step. Longer and thinner bridges can collapse due to electrostatic force between the transmission line and the bridge metal sheet.
All the lithography process steps were carried out by using e-beam lithography.

6.2.3 Characteristics of GFET IC amplifiers

Fig. 6.5 shows the equivalent circuit of the GFET IC amplifiers including three inductors, two capacitors and a GFET. The values of the passive components are given in the Table 6.2. The gain of the amplifier is measured and characterised as the transducer power gain, which at a certain bias conditions is given as:

$$G_T = \frac{1- \mid \Gamma_S \mid^2}{\mid 1 - \Gamma_{in}\Gamma_S \mid^2} \mid S_{21} \mid^2 \frac{1- \mid \Gamma_L \mid^2}{\mid 1 - S_{22}\Gamma_L \mid^2} \tag{6.1}$$

where Γ_{in} is the input reflection coefficient presented by the amplifier design and Γ_S, Γ_L are the source and load reflection coefficient when looking from the device toward the load and the source. After implementing the matching circuit, the gain of the amplifier is $\mid S_{21} \mid^2$. Fig. 6.6 shows the performance of the fully integrated 15 GHz GFET amplifier. The stability constant calculated

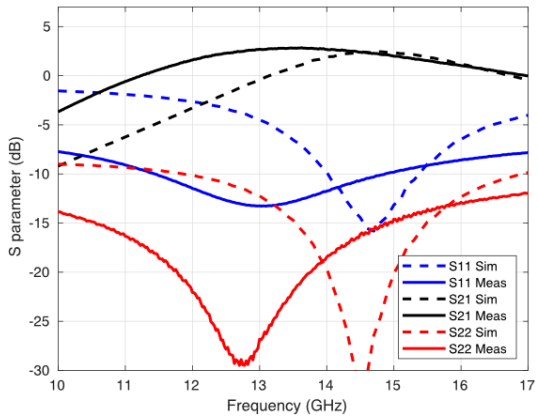


Figure 6.6: Simulated and measured S-parameters of the 15 GHz GFET IC amplifier.

from the measured S-parameters indicates that the GFET IC amplifiers are unconditionally stable. The plots shows the simulated and measured S-parameters obtained at V_G=-0.5 V and V_D=-1.27 V. From 11.4 GHz to 15 GHz measured $|S_{11}|$ and $|S_{22}|$ are below -10 dB. A measured peak gain of 2.9 dB was achieved at 13.6 dB. The difference in the simulated and measured gain is discussed and explained in the Paper [G].

Chapter 7

Conclusions and future outlook

The objective of this journey was to enhance the high frequency performance of GFETs via better understanding and getting rid of the technology limitations. To achieve this objective, the following tasks were carried out: modelling and optimization; design and technology development; fabrication of devices; DC and RF characterisation and performance analysis. The main achievements of this thesis work are as follows.

A novel fabrication technique was developed and optimized, in which a protective dielectric layer, Al_2O_3 or TiO_2, was formed on top of graphene at initial stages of the device fabrication. This allows for encapsulation of graphene, which preserves the intrinsic graphene quality and, simultaneously provides high quality metal-graphene junctions with low contact resistance. This fabrication process allowed for remarkable improvement in the GFET performance with reproducible results.

The correlations between graphene/dielectric material quality, small-signal equivalent circuit parameters and high-frequency FOMs of GFETs have been studied and reported in Paper [A]. A novel approach in analysis of the correlations was applied, which allowed for identifying the dominant limitations of the high-frequency performance of transistors and clarified the paths for future technology development. It was found, that the relatively high-drain conductance, which is currently the main limiting factor, can be counterbalanced by higher transconductance via increasing the carrier velocity. Contrary to previous reports, it was found that the contact resistance, reduced significantly in the developed technology, has a minor effect on the GFET high-frequency performance. Analysis indicated that the GFET high-frequency performance can be further enhanced by utilising the gate and substrate dielectric materials with higher OP energies, allowing for higher saturation velocity and, hence, higher f_{T} and f_{max}.

The GFETs with state-of-the-art high-frequency performance were developed and presented in Paper [B], revealing the high extrinsic $f_{\mathrm{T}} = 34$ GHz and $f_{\mathrm{max}} = 37$ GHz at L = 0.5 μm along with improved scaling behaviour. The improvement is achieved via using high quality graphene, as well as due to extremely low source/drain contact resistance and low drain conductance

as a result of better drain current saturation. As a result of analysis, it was suggested replacing the SiO_2 by Al_2O_3, i.e. material with higher OPs energy.

The above proposal was experimentally verified via encapsulating the graphene channel by Al_2O_3 layers inserting one as a buffer between the graphene and substrate. The Al_2O_3 has 30% higher OP energy than that of SiO_2. As shown in Paper [C], the GFETs with the Al_2O_3 buffer layer revealed extrinsic f_T and f_{max} up to 43 and 46 GHz, respectively, at 0.5 μm gate length, which were 30% higher than the best published f_T and f_{max} for GFETs with similar gate length.

As a further step, GFETs on a diamond, material with even higher OP energy of 165 meV, were developed, fabricated and presented in Paper [D]. The GFETs on diamond demonstrated the state-of-the-art f_{max} up to 60 GHz at gate length of 0.5 μm. The high thermal conductivity of diamond provides an efficient heat-sink, and its relatively high OP energy allowed for increase in the saturation velocity of carriers in the graphene channel up to the intrinsic graphene value. Additionally, it was shown that GFETs on diamond, exhibit excellent scaling down behaviour.

A comprehensive theoretical analysis of the charge carrier transport in GFETs and corresponding dc and RF performance, was done, for the first time, using the self-consistent simulator based on conventional drift-diffusion model and 2D Passion's equations, and presented in Paper [E]. It was found that, at high drain fields, the high-frequency performance of GFETs is defined by a balance between mechanisms of self-heating and carrier velocity saturation.

For accurate extraction of mobility and series resistance, a parameter extraction method was developed and presented in Paper [F]. This allowed for separating information about mobility degradation and series resistance via analysis of a set of GFETs with different channel lengths and using first-order mobility degradation model.

Finally, the GFETs with enhanced high-frequency performance developed and presented in Papers [A]-[C] were implemented for designing and fabricating the X and Ku band GFET IC amplifiers. The technology of the IC passive components, including integrated capacitances, vias and air-bridges, was developed as well. As it is shown in Paper [G], the peak gain of 4.2 dB and 2.9 dB at 10.6 GHz and 13.6 GHz was measured, respectively, for the X and Ku band GFET amplifiers, which are highest reported so far for the IC GFET amplifiers in the similar frequency range.

Analysis indicates, that the future progress in development of the GFETs with competitive high-frequency performance should rely on continuing getting rid of the extrinsic limitations in the charge carrier transport in combination with aggressive scaling down of the gate length. The latter requires development and implementation of the self-aligned T-shape gate technology allowing for scaling the gate length down to deep sub-micron range.

Currently, the high-frequency performance of RF GFET is limited also by the relatively low quality of graphene and adjacent dielectrics resulting in degradation of the low-field mobility. A promising way to overcome this limitation is to completely surround the graphene channel by the high quality hBN layers, material with relatively high OP energy of 100 meV. This approach is challenging because of difficulty of manufacturing of the large area high quality hBN layers. Therefore, in order to fully exploit the unique property of

graphene of extremely high mobility and carrier velocity, considerable efforts are required for development of in-situ growth of hBN/graphene/hBN and/or similar heterostrutures, which may allow for preserving the intrinsic graphene quality. Simultaneously, the GFETs utilising CVD graphene can be developed via replacing the bottom and top gate dielectric by diamond and/or diamond-like-carbon materials. For instance, a recent development of the direct growth of graphene on diamond, which is a combination of sp2-on-sp3 technology, makes it possible not only realisation of the group IV heterostructures but also wafer-scale fabrications, and hence, making diamond substrate a promising choice for future graphene high-frequency electronics applications.

In conclusion, the efforts made in this thesis work allowed for development of the GFETs with state-of-the-art high-frequency performance, better that that of the best published GFETs and Si MOSFETs counterparts. Comprehensive analysis of the intrinsic and extrinsic limitations of the graphene properties allowed for better understanding and developing a strategy for addressing the limitations, which clarified the ways of further development and enhancing the high-frequency performance of GFETs up to the level or even higher than that of the modern III-V semiconductor transistors.

Chapter 8

Summary of appended papers

In this chapter appended papers, on which basis the thesis is composed, are summarized as follows:

Paper A

The dependence of the high-frequency performance of graphene field-effect transistors on material quality

In this paper, a novel approach of analysis of correlations between high-frequency performance of GFETs and material quality characterised by low-field mobility is demonstrated. The dependences between high-frequency FOMs, f_{T}, f_{max}, and low-field mobility were observed, explained and analysed using combined models of the small-signal equivalent circuit, drain resistance, drift velocity and saturation velocity.

My contributions: optimization and characterisation of devices, systematization of the data, analysis and interpretation of the results, paper writing together with co-authors.

Paper B

Graphene field-effect transistors with high extrinsic f_{T} and f_{max}

In this paper, the state-of-the-art GFETs with enhanced extrinsic f_{T} and f_{max} up to 34 GHz and 37 GHz, respectively, at 0.5 μm gate length, are presented. The improvement was achieved as a result of using the high quality graphene and with extremely low source/drain contact resistance.

My contributions: optimization and characterisation of the devices, systematization of the data, analysis and interpretation of the results.

Paper C

Enhanced high-frequency performance of top-gated graphene FETs due to substrate-induced improvements in charge carrier saturation velocity

This paper reports on enhancement in f_T and f_{max} of GFETs achieved via surrounding the graphene channel by layers of dielectric materials with relatively high OP energy. The GFETs were fabricated on SiO_2/Si substrates with and without a buffer layer of Al_2O_3, a material with about 30% higher optical phonon energy than that of SiO_2. The f_T and f_{max} of 43 and 46 GHz, respectively, at 0.5 μm gate length, were observed in GFETs with Al_2O_3 buffer layers. These values are approximately 30% higher than those of the GFETs without the Al_2O_3 buffer.

My contributions: Initiating the work, designing, fabrication and characterisation of the devices, analysis and interpretation of the results, and paper writing together with co-authors.

Paper D

Graphene FET on diamond for high frequency electronics

This paper reports on first GFETs on a diamond substrate with state-of-the-art f_{max} up to 60 GHz at gate length of 0.5 μm. It was experimentally demonstrated that the relatively high OP energy in diamond allows for increasing the saturation velocity of carriers in the graphene channel. The high thermal conductivity of diamond allows for avoiding the performance degradation due to self-heating. Moreover, it was shown that GFETs on diamond, exhibit excellent scaling behaviour.

My contributions: introducing the idea and initiating the work, designing, fabrication and characterisation of the devices, analysis and interpretation of the results, paper writing together with co-authors.

Paper E

Does carrier velocity saturation help to enhance f_{max} in graphene field-effect transistors?

This paper describes the comprehensive theoretical analysis of high-frequency performance of GFETs in corellation with material quality made via applying models of drain resistance, carrier velocity and saturation velocity. Main results allowed for identifying the limitations and proposing approaches most promising for further development of the GFETs suitable for advanced high-frequency applications.

My contributions: optimization and characterisation of the device, systematization of the data, analysis and interpretation of the results.

Paper F

Mobility Degradation and Series Resistance in Graphene Field-Effect Transistors

In this paper, a first-order mobility degradation model is presented and used to separate the information about mobility degradation and series resistance for a set of top-gated GFETs of different channel lengths. A mobility degradation behaviour was observed with the mobility being reduced to half as the voltage-induced charge carrier density reaches to 10^{13} cm^{-2}.

My contributions: designing, fabrication and characterisation of the devices, analysis and plotting the results.

Paper G

Integrated 10-GHz Graphene FET Amplifier

This paper reports on design, fabrication and characterisation of a GFET IC amplifiers operating in X and Ku bands. The IC passives including thin film capacitors, air bridges, and loop inductors were also developed and realised. A gain of 4.2 dB at 10.6 GHz was measured for a single transistor amplifier stage and agrees well with simulations.

My contributions: fabrication and characterisation of the devices, analysis and interpretation of the results, paper writing together with co-authors.

Chapter 9

Appendix

9.1 S-parameter measurements

The set-up used for S-parameters measurements consists of three basic components, a vector network analyzer (VNA), a source-meter and under-test device. The VNA used in this work was a Agilent N5230A network analyzer with frequency range of 10 MHz to 50 GHz. For dc biasing, a dual channel Keithley source-meter was connected to VNA through an external bias-tee. The device under-test was connected to VNA using probe-station containing ground-signal-ground (GSG) probe with a pitch of 100 μm which was suitable for GFET measurement contact pad designed in this work. The S-parameters of GFET were mostly measured by sweeping the frequency ranging from 1 GHz up to above 30 GHZ using a -10 dBm microwave power.

However, before starting the measurements, two-port open, short, load and thru (SOLT) calibrations were performed using a standard calibration chip. The calibration was necessary to set-up the 50 Ω reference planes at the GSG probe tips and to remove the affect cables and probes impedance. The S-parameters was measured by sweeping the biasing conditions, i.e., combination of the gate-source voltage (V_{G}) and the drain voltage (V_{D}) in order to see and optimise the GFET high-frequency performance i.e. the highest f_{T} and f_{max}. The dual channel source meter was serving the biasing sweeping as well as for recording the IV measurements while measuring the S-parameters.

9.2 De-embedding

On-chip measurement is necessary for testing and analysing the device performance. For this purpose, large metal pad designed and fabricated along with the transistor. The metal pad embedded in the transistor and the associated lumped elements can be seen in the Fig. 9.1 (a) and (b), respectively. In order to get the real extrinsic GFET device, the lumped elements associated with the measurement pad is indeed needed to remove. The lumped elements can be removed by first measuring the S-parameters of the open and short test structure and then follow the standard de-embedding method [96]. Fig. 9.1 (c) show the original GFET without the pads and its equivalent circuit after de-

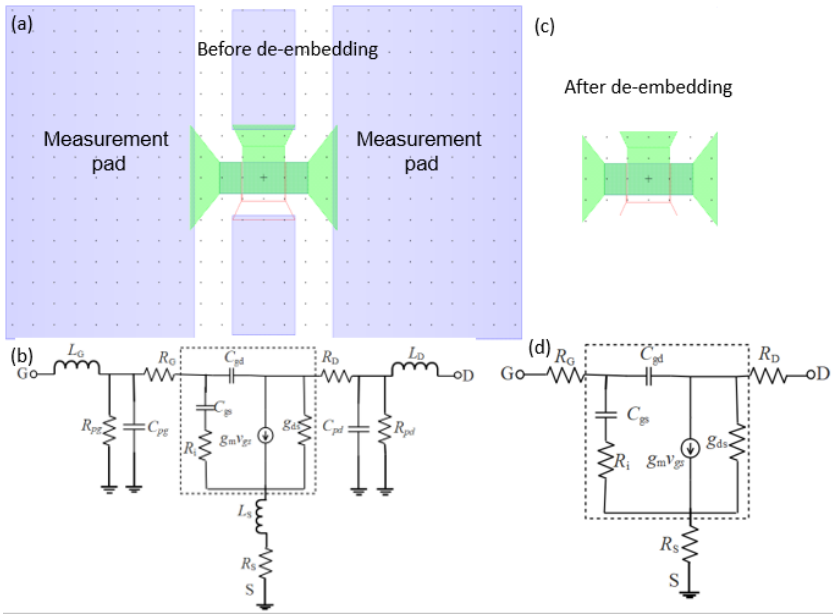


Figure 9.1: (a) Original GFET designed showing the measuring pad (b) small-signal equivalent circuit of GFET with pad before de-embedding (c) schematic showing the GFET after de-embedding (d) small-signal equivalent circuit of GFET after de-embedding.

embedding in (d). In some case, to analyse the intrinsic GFET high-frequency performance remaining extrinsic circuit components can also be removed using the same de-embedding approach.

9.3 Figures of merit of RF GFETs

The figures of merits of high-frequency transistors are the transit frequency f_T and the maximum frequency of oscillation f_{max} and their values are served for bench marking the high-frequency performance. The f_T is the frequency at which current gain h_{21} drops to unity, and the f_{max} is the frequency at which unilateral power gain (Mason's gain) U is equal to unity [94]. Both f_T and f_{max} can be directly extracted from the S-parameter measurements. The expressions for current gain and unilateral Mason's gain in terms of S-parameters are:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{9.1}$$

$$U = \frac{|\, S_{12} - S_{21} \,|^2}{det(1 - SS^*)} \tag{9.2}$$

9.4 Fabrication of GFETs and passive IC components

1. Evaporation of Al seed layer
a) Evaporate 1 nm Al in LESKER1

b) Put it on hotplate for 5 min at 160 °C
c) Repeat a)-b) 4 times
2. Marks lithography
a) Spin MMA (8.5) EL10, 1 min, 3000 rpm (400 nm) and bake 5 min on hotplate at 160 °C
b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (150 nm) and bake 5 min on hotplate at 160 °C
c) E-Beam with dose 350 and 35nAap
d) Developer: 1. n-Amylacetate 45 sec + blow dry with N_2, 2. MIBK:IPA 1:1 120 sec + blow dry with N_2
e) Remove resist with plasma etching (RIE)
f) Remove Al_2O_3 in 1:10 BOE:H20 for 5 sec.
g) Remove graphene with RIE
h) Evaporate Ti/Au 4 nm/70 nm
i) Lift off: acetone for 10 min at 75 °C; rinse in acetone; rinse in isopropanol
3. Mesa lithography
a) Spin man2403; 1 min; 3000 rpm (300nm)
Bake 1 min at 90 °C
b) E-Beam with dose 170, setp size 30, 10nAap7
c) Developer MF-24A; 45 sec; wash in H_2O
d) Remove resist; RIE
e) Remove Al_2O_3 in 1:10 BOE:H_2O for 5 sec.
f) Remove graphene with RIE
g) Wash off resist in acetone and isopropanol
4. Omic contact /Bottom capacitor plat lithography a) Spin MMA (8.5) EL10, 1 min, 3000 rpm (400nm) and bake 5 min on hotplate at 160 °C
b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (150nm) and bake 5 min on hotplate at 160 °C
c) E-Beam with dose 360 and 10nAap
d) Developer 1. N-Amylacetate 45 sec + blow dry with N_2, 2. MIBK:IPA 1:1 120 sec+blow dry with N_2
e) Remove Al_2O_3 in 1:10 BOE:H_2O for 5 sec.
f) Evaporate Ti/Pd/Au 1 nm/15 nm/250 nm
g) Lift off: acetone for 10 min at 75 °C; rinse in acetone; rinse in isopropanole
5. Form gate oxide a) Repeat 6x Evaporate Al 1 nm put on hotplate for 5 min at 160 C
b) ALD; thermal Al_2O_3 300 °C; 6 nm (71 cycles) total Al_2O_3 thickness 30 nm
6. Capacitors oxide thickness a) Spin MMA (8.5) EL10, 1 min, 2800 rpm (420 nm) at bake 5 min on hotplate at 160 °C
b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (150 nm) and bake 5 min on hotplate at 160 ° C
c) E-Beam with dose 360 and 10Aap7
d) Developer 1. N-Amylacetate 45 sec + blow dry with N_2
2. MIBK:IPA 1:1 120 sec+blow dry with N_2
e) Repeat 6x Evaporate Al 1 nm put on hotplate for 5 min at 160 C
7. Through/Metal pad through Lithography (contact covered with oxide can now be expose reduce a lithography step) a) Spin MMA (8.5) EL10, 1 min, 2800 rpm (420 nm) at bake 5 min on hotplate at 160 °C
b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (150 nm) and bake 5 min on hotplate

at 160 ° C
c) E-Beam with dose 360 and 10Aap7
d) Developer 1. N-Amylacetate 45 sec + blow dry with N_2
2. MIBK:IPA 1:1 120 sec+blow dry with N_2
e) Remove resist; RIE 5s f) Wet-etching for the via contact g) Evaporate Ti/Au 2nm/50nm (for accurate metal thickness think about capacitor oxide thickness) h) Lift off: acetone for 10 min @75C; rinse in acetone; rinse in isopropanole 8. Gate lithography/Top metal lithography/Inductors (expose separate steps) a) Spin MMA (8.5) EL10, 1 min, 2800 rpm (420 nm) at bake 5 min on hotplate at 160 °C
b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (150 nm) and bake 5 min on hotplate at 160 ° C
c) E-Beam with dose 390 and 10Aap7
d) Developer 1. N-Amylacetate 45 sec + blow dry with N_2
2. MIBK:IPA 1:1 120 sec+blow dry with N_2
e) Evaporate Ti/Au 10 nm/290 nm
f) Lift off: acetone for 10 min at 75 °C; rinse in acetone; rinse in isopropanole 9. Bridge lithography
a) (PDMS double layers at 100°C) PMGI, 1 min, 3000rpm (2400nm) Bake 10 min gradually from 90 to 190°C.
b) E-Beam with dose 390 and 35nAap8
c) Developer MF-319: H2O (2:1) 2min+clean with water + blow dry with N2
d) Re-flow 250°C for 30 sec
e) 1. MMA-EL13 2000rpm (850nm) bake at 160 for 5min, 2. PMMA-A6 3000rpm (500nm) bake at 170 7min
f) E-Beam with dose 645 and 10nAap7
g) Developer: 1. ISP: H2O (9:1) 50 sec + blow dry with N2, 2. MIBK: ISP (1:1) 150 sec + blow dry with N2
h) Evaporate: Ti/Au 10nm/1000 nm
i) 1. left-off Acetone (until developed completely), 2. left-off remover 1165 150sec at 85°C

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Bibliography

[1] W. Shockley, "A unipolar" field-effect" transistor," *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365–1376, 1952.

[2] "www.statista.com," Statista, Tech. Rep., 2019.

[3] T. Kurner and S. Priebe, "Towards THz communications-status in research, standardization and regulation," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 35, no. 1, pp. 53–62, 2014.

[4] D. Lie, J. Mayeda, Y. Li, and J. Lopez, "A Review of 5G Power Amplifier Design at cm-Wave and mm-Wave Frequencies," *Wireless Communications and Mobile Computing*, vol. 2018, 2018.

[5] F. Schwierz and J. J. Liou, "RF transistors: Recent developments and roadmap toward terahertz applications," *Solid-State Electronics*, vol. 51, no. 8, pp. 1079–1091, 2007.

[6] F. Schwierz, "Graphene transistors," *Nature nanotechnology*, vol. 5, no. 7, p. 487, 2010.

[7] R. Lai, X. Mei, W. Deal, W. Yoshida, Y. Kim, P. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange *et al.*, "Sub 50 nm InP HEMT device with Fmax greater than 1 THz," in *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 609–611.

[8] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb *et al.*, "Fabrication and mobility characteristics of ultra-thin strained si directly on insulator (SSDOI) MOSFETs," in *IEEE International Electron Devices Meeting 2003.* IEEE, 2003, pp. 3–1.

[9] A. A. Abidi, "RF-CMOS comes of age," *IEICE transactions on electronics*, vol. 87, no. 6, pp. 840–853, 2004.

[10] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *science*, vol. 306, no. 5696, pp. 666–669, 2004.

[11] K. S. Novoselov, D. Jiang, F. Schedin, T. Booth, V. Khotkevich, S. Morozov, and A. K. Geim, "Two-dimensional atomic crystals," *Proceedings of the National Academy of Sciences*, vol. 102, no. 30, pp. 10 451–10 453, 2005.

[12] A. C. Ferrari, F. Bonaccorso, V. FalKo, K. S. Novoselov, S. Roche, P. Bolggild, S. Borini, F. H. Koppens, V. Palermo, N. Pugno *et al.*, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2015.

[13] K. Bolotin, K. Sikes, J. Hone, H. Stormer, and P. Kim, "Temperature-dependent transport in suspended graphene," *Physical review letters*, vol. 101, no. 9, p. 096802, 2008.

[14] L. Banszerus, M. Schmitz, S. Engels, J. Dauber, M. Oellers, F. Haupt, K. Watanabe, T. Taniguchi, B. Beschoten, and C. Stampfer, "Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper," *Science advances*, vol. 1, no. 6, p. e1500222, 2015.

[15] M. A. Yamoah, W. Yang, E. Pop, and D. Goldhaber-Gordon, "High-velocity saturation in graphene encapsulated by hexagonal boron nitride," *ACS nano*, vol. 11, no. 10, pp. 9914–9919, 2017.

[16] O. Habibpour, Z. S. He, W. Strupinski, N. Rorsman, T. Ciuk, P. Ciepielewski, and H. Zirath, "A W-band MMIC Resistive Mixer Based on Epitaxial Graphene FET," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 168–170, Feb. 2017.

[17] M. A. Andersson, Y. Zhang, and J. Stake, "A 185–215-GHz subharmonic resistive graphene FET integrated mixer on silicon," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 165–172, 2017.

[18] A. Medina-Rull, F. Pasadas, E. G. Marin, A. Toral-Lopez, J. Cuesta, A. Godoy, D. Jimeneznez, and F. G. Ruiz, "A graphene field-effect transistor based analogue phase shifter for high-frequency applications," *IEEE Access*, vol. 8, pp. 209 055–209 063, Dec. 2020.

[19] J. Lee, T.-J. Ha, K. N. Parrish, S. F. Chowdhury, L. Tao, A. Dodabalapur, and D. Akinwande, "High-performance current saturating graphene field-effect transistor with hexagonal boron nitride dielectric on flexible polymeric substrates," *IEEE electron device letters*, vol. 34, no. 2, pp. 172–174, 2013.

[20] M. E. Ramón, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Three-gigahertz graphene frequency doubler on quartz operating beyond the transit frequency," *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 877–883, 2012.

[21] A. A. Generalov, M. A. Andersson, X. Yang, A. Vorobiev, and J. Stake, "A 400-GHz graphene FET detector," *IEEE Transactions on Terahertz Science and Technology*, vol. 7, no. 5, pp. 614–616, Sep. 2017.

[22] X. Yang, A. Vorobiev, J. Yang, K. Jeppson, and J. Stake, "A Linear-Array of 300-GHz Antenna Integrated GFET Detectors on a Flexible Substrate," *IEEE Transactions on Terahertz Science and Technology*, vol. 10, no. 5, pp. 554–557, 2020.

[23] C.-Y. Fan, M.-D. Wei, B. Uzlu, Z. Wang, D. Neumaier, and R. Negra, "Fully integrated 2.4 GHz flexible rectifier using chemical-vapor-deposition graphene MMIC proces."

[24] M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier," *Electronics letters*, vol. 48, no. 14, pp. 861–863, 2012.

[25] M. Tanzid, M. Andersson, J. Sun, and J. Stake, "Microwave noise characterization of graphene field effect transistors," *Applied Physics Letters*, vol. 104, no. 1, p. 013502, 2014.

[26] J. Aguirre-Morales, S. Fregonese, A. Dwivedi, T. Zimmer, M. Khenissa, M. Belhaj, and H. Happy, "Towards amplifier design with a SiC graphene field-effect transistor," in *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*. IEEE, Jan. 2015.

[27] C. Yu, Z. Z. He, Q. B. Liu, X. B. Song, P. Xu, T. T. Han, J. Li, Z. H. Feng, and S. J. Cai, "Graphene amplifier MMIC on SiC substrate," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 684–687, May 2016.

[28] C. Yu, Z. He, X. Song, X. Gao, Q. Liu, Y. Zhang, G. Yu, T. Han, C. Liub, Z. Feng *et al.*, "Field effect transistors and low noise amplifier mmics of monolayer graphene," *IEEE Electron Device Letters*, 2020.

[29] F. Schwierz, "Graphene transistors: status, prospects, and problems," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1567–1584, 2013.

[30] I. Meric, C. R. Dean, S.-J. Han, L. Wang, K. A. Jenkins, J. Hone, and K. Shepard, "High-frequency performance of graphene field-effect transistors with saturating IV-characteristics," in *2011 International Electron Devices Meeting*. IEEE, 2011, pp. 2–1, doi:10.1109/IEDM.2011.6131472.

[31] M.-W. Lin, C. Ling, L. A. Agapito, N. Kioussis, Y. Zhang, M. M.-C. Cheng, W. L. Wang, E. Kaxiras, and Z. Zhou, "Approaching the intrinsic band gap in suspended high-mobility graphene nanoribbons," *Physical Review B*, vol. 84, no. 12, p. 125411, 2011.

[32] Y. Wu, Y.-m. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, no. 7341, p. 74, 2011.

[33] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris *et al.*, "State-of-the-art graphene high-frequency electronics," *Nano letters*, vol. 12, no. 6, pp. 3062–3067, 2012.

[34] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler *et al.*, "Record maximum oscillation frequency in C-face epitaxial graphene transistors," *Nano letters*, vol. 13, no. 3, pp. 942–947, 2013.

[35] H. Lyu, Q. Lu, J. Liu, X. Wu, J. Zhang, J. Li, J. Niu, Z. Yu, H. Wu, and H. Qian, "Deep-submicron Graphene Field-Effect Transistors with state-of-Art fmax," *Scientific reports*, vol. 6, p. 35717, 2016.

[36] E. Guerriero, P. Pedrinazzi, A. Mansouri, O. Habibpour, M. Winters, N. Rorsman, A. Behnam, E. A. Carrion, A. Pesquera, A. Centeno *et al.*, "High-gain graphene transistors with a thin Al_2O_x top-gate oxide," *Scientific reports*, vol. 7, no. 1, pp. 1–7, 2017, doi:10.1038/s41598-017-02541-2.

[37] M. Bonmann, M. A. Andersson, Y. Zhang, X. Yang, A. Vorobiev, and J. Stake, "An Integrated 200-GHz Graphene FET Based Receiver," in *2018 43rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*. IEEE, 2018, pp. 1–3.

[38] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, K. Jeppson, L. Banszerus, M. Otto, C. Stampfer, D. Neumaier, and J. Stake, "The Dependence of the High-Frequency Performance of Graphene Field-Effect Transistors on Channel Transport Properties," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 457–464, 2020.

[39] E. V. Castro, K. Novoselov, S. Morozov, N. Peres, J. L. Dos Santos, J. Nilsson, F. Guinea, A. Geim, and A. C. Neto, "Biased bilayer graphene: semiconductor with a gap tunable by the electric field effect," *Physical review letters*, vol. 99, no. 21, p. 216802, 2007.

[40] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature nanotechnology*, vol. 3, no. 11, p. 654, 2008.

[41] A. Vorobiev, M. Bonmann, M. Asad, X. Yang, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake, "Graphene field-effect transistors for millimetre wave amplifiers," *Proceeding of the IEEE*, 2019, doi:10.1109/IRMMW-THz.2019.8874149.

[42] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake, "Graphene Field-Effect Transistors With High Extrinsic ft and fmax," *IEEE Electron Device Letters*, vol. 40, no. 1, pp. 131–134, 2019.

[43] M. Asad, K. O. Jeppson, A. Vorobiev, M. Bonmann, and J. Stake, "Enhanced High-Frequency Performance of Top-Gated Graphene FETs Due to Substrate- Induced Improvements in Charge Carrier Saturation Velocity," *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 899–902, 2021.

[44] M. Bonmann, A. Vorobiev, M. A. Andersson, and J. Stake, "Charge carrier velocity in graphene field-effect transistors," *Applied Physics Letters*, vol. 111, no. 23, p. 233505, 2017.

[45] J. Lee, T.-J. Ha, H. Li, K. N. Parrish, M. Holt, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "25 GHz embedded-gate graphene transistors with high-k dielectrics on extremely flexible plastic sheets," *ACS nano*, vol. 7, no. 9, pp. 7744–7750, 2013.

[46] W. Zhu, S. Park, M. N. Yogeesh, K. M. McNicholas, S. R. Bank, and D. Akinwande, "Black phosphorus flexible thin film transistors at gighertz frequencies," *Nano letters*, vol. 16, no. 4, pp. 2301–2306, 2016.

[47] A. Sanne, S. Park, R. Ghosh, M. N. Yogeesh, C. Liu, D. Akinwande, S. K. Banerjee, L. Mathew, and R. Rao, "Record fT, fmax, and GHz amplification in 2dimensional CVD MoS2 embedded gate FETs," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2017, pp. 1–4.

[48] H. Wang, A. L. Hsu, and T. Palacios, "Graphene electronics for RF applications," *IEEE Microwave Magazine*, vol. 13, no. 4, pp. 114–125, 2012.

[49] L. Wang, I. Meric, P. Huang, L. Gao, D. Muller *et al.*, "One-dimensional electrical contact to a two-dimensional material," *Science*, vol. 342, no. 6158, pp. 614–617, 2013.

[50] I. Post, M. Akbar, G. Curello, S. Gannavaram, W. Hafez, U. Jalan, K. Komeyli, J. Lin, N. Lindert, J. Park *et al.*, "A 65nm CMOS SOC technology featuring strained silicon transistors for RF applications," in *2006 International Electron Devices Meeting*. IEEE, 2006, pp. 1–3.

[51] R. Peierls, "Quelques proprietes typiques des corps solides," in *Annales de l'institut Henri Poincare*, vol. 5, no. 3, 1935, pp. 177–222.

[52] A. K. Geim and K. S. Novoselov, "The rise of graphene," in *Nanoscience and Technology: A Collection of Reviews from Nature Journals*. World Scientific, 2010, pp. 11–19.

[53] S. Dimitrijev, *Principles of semiconductor devices*. Oxford University Press, USA, 2006.

[54] A. C. Neto, F. Guinea, N. M. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Reviews of modern physics*, vol. 81, no. 1, p. 109, 2009.

[55] S. D. Sarma, S. Adam, E. Hwang, and E. Rossi, "Electronic transport in two-dimensional graphene," *Reviews of modern physics*, vol. 83, no. 2, p. 407, 2011.

[56] V. E. Dorgan, M.-H. Bae, and E. Pop, "Mobility and saturation velocity in graphene on SiO2," *Applied Physics Letters*, vol. 97, no. 8, p. 082112, 2010.

[57] D. Caughey and R. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192–2193, 1967.

[58] J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee *et al.*, "Highly flexible and transparent multilayer MoS2 transistors with graphene electrodes," *Small*, vol. 9, no. 19, pp. 3295–3300, 2013.

[59] T. Li, M. Tian, S. Li, M. Huang, X. Xiong, Q. Hu, S. Li, X. Li, and Y. Wu, "Black phosphorus radio frequency electronics at cryogenic temperatures," *Advanced Electronic Materials*, vol. 4, no. 8, p. 1800138, 2018.

[60] K. K. Smithe, C. D. English, S. V. Suryavanshi, and E. Pop, "High-field transport and velocity saturation in synthetic monolayer MoS2," *Nano letters*, vol. 18, no. 7, pp. 4516–4522, 2018.

[61] E. Hwang and S. D. Sarma, "Acoustic phonon scattering limited carrier mobility in two-dimensional extrinsic graphene," *Physical Review B*, vol. 77, no. 11, p. 115449, 2008.

[62] E. Hwang, S. Adam, and S. D. Sarma, "Carrier transport in two-dimensional graphene layers," *Physical review letters*, vol. 98, no. 18, p. 186806, 2007.

[63] J.-H. Chen, C. Jang, S. Adam, M. Fuhrer, E. Williams, and M. Ishigami, "Charged-impurity scattering in graphene," *Nature Physics*, vol. 4, no. 5, p. 377, 2008.

[64] J.-H. Chen, C. Jang, M. Ishigami, S. Xiao, W. Cullen, E. Williams, and M. Fuhrer, "Diffusive charge transport in graphene on SiO2," *Solid State Communications*, vol. 149, no. 27-28, pp. 1080–1086, 2009.

[65] A. Matthiessen and C. Vogt, "On the influence of temperature on the electric conducting-power of alloys," *Philosophical Transactions of the Royal Society of London*, no. 154, pp. 167–200, 1864.

[66] F. Giannazzo, S. Sonde, R. L. Nigro, E. Rimini, and V. Raineri, "Mapping the density of scattering centers limiting the electron mean free path in graphene," *Nano letters*, vol. 11, no. 11, pp. 4612–4618, 2011.

[67] D. A. Neamen, *Semiconductor physics and devices: basic principles*. New York, NY: McGraw-Hill,, 2012.

[68] M. Ishigami, J. Chen, W. Cullen, M. Fuhrer, and E. Williams, "Atomic structure of graphene on SiO2," *Nano letters*, vol. 7, no. 6, pp. 1643–1648, 2007.

[69] F. Pizzocchero, L. Gammelgaard, B. S. Jessen, J. M. Caridad, L. Wang, J. Hone, P. Bøggild, and T. J. Booth, "The hot pick-up technique for batch assembly of van der waals heterostructures," *Nature communications*, vol. 7, no. 1, pp. 1–10, 2016.

[70] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. v. Smet, K. Von Klitzing, and A. Yacoby, "Observation of electron–hole puddles in graphene using a scanning single-electron transistor," *Nature physics*, vol. 4, no. 2, p. 144, 2008.

[71] D. Liu, S. Clark, and J. Robertson, "Oxygen vacancy levels and electron transport in Al2O3," *Applied physics letters*, vol. 96, no. 3, p. 032905, 2010.

[72] J. W. Suk, W. H. Lee, J. Lee, H. Chou, R. D. Piner, Y. Hao, D. Akinwande, and R. S. Ruoff, "Enhancement of the electrical properties of graphene grown by chemical vapor deposition via controlling the effects of polymer residue," *Nano letters*, vol. 13, no. 4, pp. 1462–1467, 2013.

[73] S. Adam, E. Hwang, V. Galitski, and S. D. Sarma, "A self-consistent theory for graphene transport," *Proceedings of the National Academy of Sciences*, vol. 104, no. 47, pp. 18 392–18 397, 2007.

[74] S. M. Sze, *Semiconductor devices: physics and technology, page 395-396*. John wiley & sons, 2007.

[75] K. Nummila, A. Ketterson, and I. Adesida, "Delay time analysis for short gate-length GaAs MESFETs," *Solid-state electronics*, vol. 38, no. 2, pp. 517–524, 1995.

[76] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, pp. 662–662, 2010, doi:10.1126/science.1184289.

[77] C. Virojanadara, M. Syvajarvi, R. Yakimova, L. Johansson, A. Zakharov, and T. Balasubramanian, "Homogeneous large-area graphene layer growth on 6 H-SiC (0001)," *Physical Review B*, vol. 78, no. 24, p. 245403, 2008.

[78] P. Mondelli, B. Gupta, M. G. Betti, C. Mariani, J. L. Duffin, and N. Motta, "High quality epitaxial graphene by hydrogen-etching of 3C-SiC (111) thin-film on Si (111)," *Nanotechnology*, vol. 28, no. 11, p. 115601, 2017.

[79] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc *et al.*, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *science*, vol. 324, no. 5932, pp. 1312–1314, 2009.

[80] S. Ryu, L. Liu, S. Berciaud, Y.-J. Yu, H. Liu, P. Kim, G. W. Flynn, and L. E. Brus, "Atmospheric oxygen binding and hole doping in deformed graphene on a SiO2 substrate," *Nano letters*, vol. 10, no. 12, pp. 4944–4951, 2010.

[81] A. Das, S. Pisana, U. Chakraborty, K. Novoselov, H. Krishnamurthy, A. Geim, A. Ferrari *et al.*, "Monitoring dopants by Raman scattering in an electrochemically top-gated graphene transistor," *Nature nanotechnology*, vol. 3, no. 4, pp. nnano–2008, 2008.

[82] T. Mohiuddin, A. Lombardo, R. Nair, A. Bonetti, G. Savini, R. Jalil, N. Bonini, D. Basko, C. Galiotis, N. Marzari *et al.*, "Uniaxial strain in graphene by Raman spectroscopy: G peak splitting, Grneisen parameters, and sample orientation," *Physical Review B*, vol. 79, no. 20, p. 205433, 2009.

[83] C. Casiraghi, S. Pisana, K. Novoselov, A. Geim, and A. Ferrari, "Raman fingerprint of charged impurities in graphene," *Applied Physics Letters*, vol. 91, no. 23, p. 233108, 2007.

[84] E. Koo and S.-Y. Ju, "Role of residual polymer on chemical vapor grown graphene by Raman spectroscopy," *Carbon*, vol. 86, pp. 318–324, 2015.

[85] A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. Magnuson, S. McDonnell, L. Colombo, E. Vogel, R. Ruoff, and R. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO2," *Applied Physics Letters*, vol. 99, no. 12, p. 122108, 2011.

[86] Y. Ahn, H. Kim, Y.-H. Kim, Y. Yi, and S.-I. Kim, "Procedure of removing polymer residues and its influences on electronic and structural characteristics of graphene," *Applied Physics Letters*, vol. 102, no. 9, p. 091602, 2013.

[87] M. V. Sullivan and J. H. Eigler, "Five metal hydrides as alloying agents on silicon," *Journal of The Electrochemical Society*, vol. 103, no. 4, pp. 218–220, 1956.

[88] K. Shih and J. Blum, "Contact resistances of Au Ge Ni, Au Zn and Al to III–V compounds," *Solid-State Electronics*, vol. 15, no. 11, pp. 1177–1180, 1972.

[89] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices," *IEEE Transactions on Electron Devices*, vol. 16, no. 12, pp. 1022–1024, 1969.

[90] D. K. Schroder, *Semiconductor material and device characterization*. John Wiley & Sons, 2006.

[91] M. Shaygan, M. Otto, A. A. Sagade, C. A. Chavarin, G. Bacher, W. Mertin, and D. Neumaier, "Low resistive edge contacts to CVD-grown graphene using a CMOS compatible metal," *Annalen der Physik*, vol. 529, no. 11, p. 1600410, 2017.

[92] F. Xia, V. Perebeinos, Y.-m. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal–graphene junction resistance," *Nature nanotechnology*, vol. 6, no. 3, p. 179, 2011.

[93] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric," *Applied Physics Letters*, vol. 94, no. 6, p. 062107, 2009.

[94] S. Mason, "Power gain in feedback amplifier," *Transactions of the IRE Professional Group on Circuit Theory*, no. 2, pp. 20–25, 1954.

[95] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum fT of millimeter-wave MODFETs," *IEEE Electron Device Letters*, vol. 10, no. 7, pp. 291–293, 1989.

[96] G. Dambrine, A. Cappy, F. Heliodore, E. Playez *et al.*, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on microwave theory and techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.

[97] J. Moon, H.-C. Seo, M. Antcliffe, D. Le, C. McGuire, A. Schmitz, L. Nyakiti, D. Gaskill, P. Campbell, K.-M. Lee *et al.*, "Graphene FETs for zero-bias linear resistive FET mixers," *IEEE Electron Device Letters*, vol. 34, no. 3, pp. 465–467, 2013.

[98] C. Raynaud, O. Faynot, J.-L. Pelloie, C. Tabone, A. Grouillet, F. Martin, G. Dambrine, M. Vanmackelberg, L. Picheta, E. Mackowiak *et al.*, "70 GHZ FMAX fully-depleted SOI MOSFETS for low-power wireless applications," 2000.

[99] R. A. Johnson, P. De La Houssaye, C. E. Chang, P.-F. Chen, M. E. Wood, G. A. Garcia, I. Lagnado, and P. M. Asbeck, "Advanced thin-film silicon-on-sapphire technology: microwave circuit applications," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1047–1054, 1998.

[100] P. De la Houssaye, C. Chang, B. Offord, G. Imthurn, R. Johnson, P. Asbeck, G. Garcia, and I. Lagnado, "Microwave performance of optically fabricated T-gate thin film silicon-on-sapphire based MOSFET's," *IEEE Electron Device Letters*, vol. 16, no. 6, pp. 289–292, 1995.

[101] L. Tiemeijer, H. Boots, R. Havens, A. Scholten, P. De Vreede, P. Woerlee, A. Heringa, and D. Klaassen, "A record high 150 GHz $f_{\max}$ realized at 0.18 μm gate length in an industrial RF-CMOS technology," in *International Electron Devices Meeting. Technical Digest (Cat. No. 01CH37224)*. IEEE, 2001, pp. 10–4, doi:10.1109/IEDM.2001.979471.

[102] M.-H. Bae, S. Islam, V. E. Dorgan, and E. Pop, "Scaling of high-field transport and localized heating in graphene transistors," *ACS nano*, vol. 5, no. 10, pp. 7936–7944, 2011.

[103] M. Bonmann, M. Krivic, X. Yang, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake, "Effects of Self-Heating on f_{T} and $f_{\max}$ Performance of Graphene Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 1277–1284, 2020, doi:10.1109/TED.2020.2965004.

[104] B. Son, H. Kim, H. Jeong, J.-Y. Park, S. Lee, and Y. Ahn, "Electron beam induced removal of PMMA layer used for graphene transfer," *Scientific reports*, vol. 7, no. 1, p. 18058, 2017.

[105] O. Habibpour, J. Vukusic, and J. Stake, "A large-signal graphene FET model," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 968–975, 2012, doi:10.1109/TED.2012.2182675.

[106] H. Lyu, Q. Lu, Y. Huang, T. Ma, J. Zhang, X. Wu, Z. Yu, W. Ren, H.-M. Cheng, H. Wu *et al.*, "Graphene distributed amplifiers: Generating desirable gain for graphene field-effect transistors," *Scientific reports*, vol. 5, no. 1, pp. 1–7, 2015.

[107] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, and R. Negra, "Metal–insulator–graphene diode mixer based on CVD graphene-on-glass," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 1104–1107, 2018.

[108] A. Darwish, A. J. Bayba, and H. A. Hung, "Channel temperature analysis of gan hemts with nonlinear thermal conductivity," *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 840–846, 2015.

[109] A. A. Balandin, "Thermal properties of graphene and nanostructured carbon materials," *Nature materials*, vol. 10, no. 8, pp. 569–581, 2011.

[110] T. Kiuru, J. Mallat, A. V. Raisanen, and T. Narhi, "Schottky diode series resistance and thermal resistance extraction from *S*-parameter and temperature controlled I–V measurements," *IEEE transactions on microwave theory and techniques*, vol. 59, no. 8, pp. 2108–2116, 2011.

[111] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—a review," *IEEE transactions on power electronics*, vol. 27, no. 6, pp. 3081–3092, 2011.

[112] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, and W. Haensch, "Graphene radio frequency receiver integrated circuit," *Nature communications*, vol. 5, p. 3086, 2014.

[113] J. Chauhan and J. Guo, "High-field transport and velocity saturation in graphene," *Applied Physics Letters*, vol. 95, no. 2, p. 023120, 2009.

[114] Z. Cheng, Q. Zhou, C. Wang, Q. Li, C. Wang, and Y. Fang, "Toward intrinsic graphene surfaces: a systematic study on thermal annealing and wet-chemical treatment of SiO2-supported graphene devices," *Nano letters*, vol. 11, no. 2, pp. 767–771, 2011.

[115] C. A. Chavarin, A. A. Sagade, D. Neumaier, G. Bacher, and W. Mertin, "On the origin of contact resistances in graphene devices fabricated by optical lithography," *Applied Physics A*, vol. 122, no. 2, p. 58, 2016.

[116] S. Adam, E. Hwang, and S. D. Sarma, "Scattering mechanisms and Boltzmann transport in graphene," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 40, no. 5, pp. 1022–1025, 2008.

[117] N. Peres, F. Guinea, and A. C. Neto, "Electronic properties of disordered two-dimensional carbon," *Physical Review B*, vol. 73, no. 12, p. 125411, 2006.

[118] S. Fratini and F. Guinea, "Substrate-limited electron dynamics in graphene," *Physical Review B*, vol. 77, no. 19, p. 195415, 2008.

[119] T. Wehling, S. Yuan, A. Lichtenstein, A. Geim, and M. Katsnelson, "Resonant scattering by realistic impurities in graphene," *Physical review letters*, vol. 105, no. 5, p. 056802, 2010.

[120] T. Ando, "Screening effect and impurity scattering in monolayer graphene," *Journal of the Physical Society of Japan*, vol. 75, no. 7, pp. 074 716–074 716, 2006.

[121] J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. W. Magnuson, R. S. Ruoff, L. Colombo, R. M. Wallace, and E. M. Vogel, "Reducing extrinsic performance-limiting factors in graphene grown by chemical vapor deposition," *ACS nano*, vol. 6, no. 4, pp. 3224–3229, 2012.

[122] F. Giannazzo, S. Sonde, V. Raineri, and E. Rimini, "Irradiation damage in graphene on SiO2 probed by local mobility measurements," *Applied Physics Letters*, vol. 95, no. 26, p. 263109, 2009.

[123] J. Chauhan and J. Guo, "Inelastic phonon scattering in graphene FETs," *IEEE trans. on electron devices*, vol. 58, no. 11, pp. 3997–4003, 2011, doi:10.1109/TED.2011.2164253.

[124] M. Fischetti, D. Neumayer, and E. Cartier, "Effective electron mobility in Si inversion layers in MOS systems with a high-k insulator: The role of remote phonon scattering," *Journal of Applied Physics*, vol. 90, no. 9, p. 4587, 2001, doi:10.1063/1.1405826.

[125] J. Gun Oh, S. Ki Hong, C.-K. Kim, J. Hoon Bong, J. Shin, S.-Y. Choi, and B. Jin Cho, "High performance graphene field effect transistors on an aluminum nitride substrate with high surface phonon energy," *Applied Physics Letters*, vol. 104, no. 19, p. 193112, 2014.

[126] M. Washington and H. Cummins, "Linewidth of the sharp two-phonon raman peak in diamond," *Physical Review B*, vol. 15, no. 12, p. 5840, 1977.

[127] J. Kulda, B. Dorner, B. Roessli, H. Sterner, R. Bauer, T. May, K. Karch, P. Pavone, and D. Strauch, "A neutron-scattering study of the overbending of the [100] LO phonon mode in diamond," *Solid state communications*, vol. 99, no. 11, pp. 799–802, 1996.

[128] P. C. Feijoo, F. Pasadas, M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto *et al.*, "Does carrier velocity saturation help to enhance fmax in graphene field-effect transistors?" *Nanoscale Advances*, vol. 2, no. 9, pp. 4179–4186, 2020.

[129] J. Yu, G. Liu, A. V. Sumant, V. Goyal, and A. A. Balandin, "Graphene-on-diamond devices with increased current-carrying capacity: carbon sp2-on-sp3 technology," *Nano letters*, vol. 12, no. 3, pp. 1603–1608, 2012.

[130] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proceedings of the National Academy of Sciences*, vol. 109, no. 29, pp. 11 588–11 592, 2012.

[131] Z. Wang, S. Liang, Z. Zhang, H. Liu, H. Zhong, L.-H. Ye, S. Wang, W. Zhou, J. Liu, Y. Chen *et al.*, "Scalable fabrication of ambipolar transistors and radio-frequency circuits using aligned carbon nanotube arrays," *Advanced Materials*, vol. 26, no. 4, pp. 645–652, 2014.

[132] H.-Y. Chang, M. N. Yogeesh, R. Ghosh, A. Rai, A. Sanne, S. Yang, N. Lu, S. K. Banerjee, and D. Akinwande, "Large-Area Monolayer MoS2 for

Flexible Low-Power RF Nanoelectronics in the GHz Regime," *Advanced materials*, vol. 28, no. 9, pp. 1818–1823, 2016.

[133] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande *et al.*, "Radio frequency transistors and circuits based on CVD MoS2," *Nano letters*, vol. 15, no. 8, pp. 5039–5045, 2015.

[134] C. Rutherglen, A. A. Kane, P. F. Marsh, T. A. Cain, B. I. Hassan, M. R. AlShareef, C. Zhou, and K. Galatsis, "Wafer-scalable, aligned carbon nanotube transistors operating at frequencies of over 100 GHz," *Nature Electronics*, vol. 2, no. 11, pp. 530–539, 2019.

[135] Z. Feng, C. Yu, J. Li, Q. Liu, Z. He, X. Song, J. Wang, and S. Cai, "An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors," *Carbon*, vol. 75, pp. 249–254, 2014.

[136] M. Steiner, M. Engel, Y.-M. Lin, Y. Wu, K. Jenkins, D. B. Farmer, J. J. Humes, N. L. Yoder, J.-W. T. Seo, A. A. Green *et al.*, "High-frequency performance of scaled carbon nanotube array field-effect transistors," *Applied Physics Letters*, vol. 101, no. 5, p. 053123, 2012.

[137] J. Wu, L. Jiao, A. Antaris, C. L. Choi, L. Xie, Y. Wu, S. Diao, C. Chen, Y. Chen, and H. Dai, "Self-assembly of semiconducting single-walled carbon nanotubes into dense, aligned rafts," *small*, vol. 9, no. 24, pp. 4142–4148, 2013.

[138] D. Zhong, H. Shi, L. Ding, C. Zhao, J. Liu, J. Zhou, Z. Zhang, and L.-M. Peng, "Carbon nanotube film-based radio frequency transistors with maximum oscillation frequency above 100 GHz," *ACS applied materials & interfaces*, vol. 11, no. 45, pp. 42 496–42 503, 2019.

[139] A. Leuther, A. Tessmann, H. Massler, R. Losch, M. Schlechtweg, M. Mikulla, and O. Ambacher, "35 nm metamorphic HEMT MMIC technology," in *2008 20th International Conference on Indium Phosphide and Related Materials*. IEEE, 2008, pp. 1–4.

[140] A. Leuther, S. Koch, A. Tessmann, I. Kallfass, T. Merkle, H. Massler, R. Loesch, M. Schlechtweg, S. Saito, and O. Ambacher, "20 nm metamorphic HEMT with 660 GHz Ft," in *IPRM 2011-23rd International Conference on Indium Phosphide and Related Materials*. IEEE, 2011, pp. 1–4.

[141] E.-Y. Chang, C.-I. Kuo, H.-T. Hsu, C.-Y. Chiang, and Y. Miyamoto, "Inas thin-channel high-electron-mobility transistors with very high current-gain cutoff frequency for emerging submillimeter-wave applications," *Applied Physics Express*, vol. 6, no. 3, p. 034001, 2013.

[142] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 547–549, 2009.

[143] O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland, and J. Stake, "A subharmonic graphene FET mixer," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 71–73, 2011.

[144] M. Asad, K. O. Jeppson, A. Vorobiev, M. Bonmann, and J. Stake, "Enhanced High-Frequency Performance of Top-Gated Graphene FETs Due to Substrate- Induced Improvements in Charge Carrier Saturation Velocity," *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 899–902, 2021.

[145] O. Habibpour, N. Rorsman, and H. Zirath, "Developing graphene based MMICs on SiC substrate," in *2015 Asia-Pacific Microwave Conference (APMC)*, vol. 1. IEEE, 2015, pp. 1–3.

[146] J. D. Aguirre-Morales, S. Frégonèse, A. D. D. Dwivedi, T. Zimmer, M. Khenissa, M. Belhaj, and H. Happy, "Towards amplifier design with a SiC graphene field-effect transistor," in *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon.* IEEE, 2015, pp. 93–96.

[147] S. F. Chowdhury, M. N. Yogeesh, S. K. Banerjee, and D. Akinwande, "Black phosphorous thin-film transistor and RF circuit applications," *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 449–451, 2016.

[148] M. Medley and J. Allen, "Broad-Band GaAs FET Amplifier Design Using Negative-Image Device Models," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 9, pp. 784–788, Sep. 1979.

[149] N.-T. Kim and O. M. Ramahi, "Power-amplifier design using negative-image device models," *Microwave and Optical Technology Letters*, vol. 47, no. 2, pp. 197–201, 2005.

Paper A

The dependence of the high-frequency performance of graphene field-effect transistors on channel transport properties

M. Asad, M. Bonmann, X. Yang, A. Vorobiev, K. Jeppson, L. Banszerus, M. Otto, C. Stampfer, D. Neumaier and J. Stake

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Paper B

Graphene field-effect transistors with high extrinsic f_{T} and f_{max}

M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier and J. Stake

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Paper C

Enhanced high-frequency performance of top-gated graphene FETs due to substrate-induced improvements in charge carrier saturation velocity

M. Asad, K. Jeppson, A. Vorobiev, M. Bonmann and J. Stake

***IEEE Transactions on Electron Devices,* 68, 899-902, 2021.**

Paper D

Graphene FET on diamond for high frequency electronics

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Manuscript, May 2021.

Paper E

Does carrier velocity saturation help to enhance $f_{\max}$ in graphene field-effect transistors?

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Paper F

Mobility degradation and series resistance in graphene field-effect transistor

K. Jeppson, M. Asad, J. Stake

IEEE Transactions on Electron Devices, 2021.

Paper G

Integrated 10-GHz Graphene FET Amplifier

A. Gareeb, M. Asad, M. -D .Wei, A. Vorobiev, J. Stake and R. Negra

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